

(19)



Europäisches Patentamt

European Patent Office

Office européen des brevets



(11)

EP 1 017 081 A2

(12)

EUROPEAN PATENT APPLICATION

(43) Date of publication:

05.07.2000 Bulletin 2000/27

(51) Int Cl.7: H01J 17/49

(21) Application number: 99126025.8

(22) Date of filing: 27.12.1999

(84) Designated Contracting States:

AT BE CH CY DE DK ES FI FR GB GR IE IT LI LU
MC NL PT SE

Designated Extension States:

AL LT LV MK RO SI

(30) Priority: 28.12.1998 JP 37312998

26.04.1999 JP 11770199

26.05.1999 JP 14637399

(71) Applicant: Pioneer Corporation

Meguro-ku, Tokyo (JP)

(72) Inventors:

- Koshio, Chiharu, c/o Pioneer Corporation
Nakakoma-gun, Yamanashi-ken 409-3843 (JP)

• Amemiya, Kimio, c/o Pioneer Corporation

Nakakoma-gun, Yamanashi-ken 409-3843 (JP)

• Komaki, Toshihiro, c/o Pioneer Corporation

Nakakoma-gun, Yamanashi-ken 409-3843 (JP)

• Taniguchi, Hitoshi, c/o Pioneer Corporation

Nakakoma-gun, Yamanashi-ken 409-3843 (JP)

• Sakai, Tatsuro, c/o Pioneer Corporation

Nakakoma-gun, Yamanashi-ken 409-3843 (JP)

• Masuda, Kosuke, c/o Pioneer Corporation

Nakakoma-gun, Yamanashi-ken 409-3843 (JP)

(74) Representative:

Bohnenberger, Johannes, Dr. et al

Meissner, Bolte & Partner

Postfach 86 06 24

81633 München (DE)

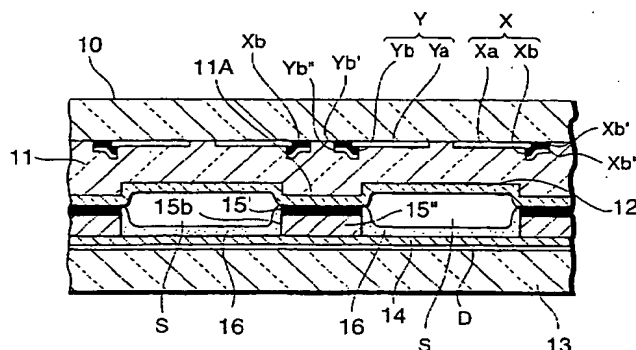
(54) Plasma display panel

(57) A plasma display panel comprises a front substrate (10) and a rear substrate (13), a plurality of row electrode pairs (X, Y) provided on the inner surface of the front substrate (10), a dielectric layer (11) provided on the inner surface of the front substrate (10) for covering the row electrode pairs (X, Y), a plurality of column electrodes (D) provided on the inner surface of the rear substrate (13), a partition wall assembly (15) provided between the front substrate (10) and the rear substrate

(13), said partition wall assembly (15) including a plurality of longitudinal partition walls (15a) and a plurality of lateral partition walls (15b), forming a plurality of discharge cells (C). In particular, the dielectric layer (11) has a plurality of projection portions (11A) located corresponding to and protruding toward the lateral partition walls (15b) of the partition wall assembly (15), in a manner such that there would be no slots formed between the dielectric layer (11) and the lateral partition walls (15b).

Fig. 2

V1-V1 SECTION



Description

BACKGROUND OF THE INVENTION

[0001] The present invention relates to a surface discharge type AC-driven plasma display panel, particularly to the discharge cell structure of such plasma display panel.

[0002] Recently, there has been appeared in the market a new type of display device which is large in size and small in thickness, with one example being a surface discharge type AC-driven plasma display panel.

[0003] Fig. 47 is a plane view schematically indicating a surface discharge type AC-driven plasma display panel made according to a prior art. Fig. 48 is a sectional view taken along line V - V in Fig. 47, Fig. 49 is a sectional view taken along line W - W in Fig. 47.

[0004] As shown in Figs. 47 - 49, the conventional plasma display panel has a front glass substrate 1 (serving as a displaying surface), a plurality of row electrode pairs (X', Y'), a dielectric layer 2 covering the row electrode pairs (X', Y'), a protection layer 3 consisting of MgO covering the dielectric layer 2.

[0005] Referring to Fig. 47, each row electrode pair (X', Y') includes a pair of transparent electrodes (Xa', Ya') consisting of ITO transparent electrically conductive film and having a relatively large width, and a pair of bus electrodes (Xb', Yb') consisting of a metal film having a relatively small width. The bus electrodes (Xb', Yb') are provided to compensate for the electric conductivity of the transparent electrodes (Xa', Ya').

[0006] Further, two row electrodes forming each row electrode pair (X', Y') are arranged in parallel with each other, forming a discharge gap g' therebetween, thereby forming one displaying line L for the plasma display panel (matrix display).

[0007] Referring to Figs. 48 and 49, the conventional plasma display panel has a rear glass substrate 4 arranged space-apart from the front glass substrate 1, thereby forming an electric discharge space S' therebetween. Further, the display panel includes a plurality of column electrodes D' arranged orthogonal to the row electrodes (X', Y'), a plurality of belt-like partition walls 5 provided between and in parallel with the column electrodes D', a fluorescent layer 6 including three kinds of original color portions 6(R), 6(G), 6(B). In detail, the fluorescent layer 6 is so provided that it covers the side surfaces of the partition walls 5 and the column electrodes D'.

[0008] In this way, the row electrode pairs (X', Y') are intersected with the column electrodes D', while the discharge space S' is divided by the partition walls 5 into a plurality of smaller sections, thereby forming a plurality of electric discharge cells C' serving as a plurality of light emission units, as shown in Fig. 47.

[0009] A displaying process of the surface discharge type AC-driven plasma display panel having the structure shown in Figs. 47 - 48 will be described in the following.

[0010] At first, an addressing operation is conducted so that an electric discharge is effected selectively among the discharge cells C' between the row electrode pairs (X', Y') and the column electrodes D'. As a result, a plurality of lit-up cells (discharge cells C' where wall charges have been formed in the dielectric layer 2) and a plurality of extinguished cells (discharge cells C' where wall charges are not formed in the dielectric layer 2) are distributed on the panel corresponding to a picture to be displayed.

[0011] Subsequently, discharge sustaining pulses are simultaneously applied to all the displaying lines L in a manner such that the row electrode pairs (X', Y') will alternatively receive the discharge sustaining pulses. In this manner, surface discharge phenomenon will occur in lit-up cells once the discharge sustaining pulses are applied thereto.

[0012] At this moment, since ultraviolet light will be generated due to the surface discharge in the lit-up cells, the fluorescent layer 6 (R, G, B) will be excited to effect light emission, thereby displaying a picture on the plasma display panel.

[0013] In the above-described surface discharge type AC-driven plasma display panel, since a fluorescent layer 6 has been provided to cover not only the column electrodes D' but also the side faces of the belt-like partition walls 5, a light emission area within each discharge cell C' has been increased, thus increasing the brightness of a picture being displayed on the panel.

[0014] However, with the above-described surface discharge type AC-driven plasma display panel, if it is desired to improve the fineness of a displayed picture by reducing the size of each discharge cell C', a total surface area of the fluorescent layer 6 will also be undesirably reduced, resulting in a deterioration in the brightness of the displayed picture.

[0015] To cope with the above problem, it is allowed to consider making narrow the pitch between each row electrode pair (X', Y'). This, however, would cause a problem called discharge interference between every two adjacent discharge cells C', hence resulting in some misdischarges.

SUMMARY OF THE INVENTION

[0016] It is a first object of the present invention to provide an improved plasma display panel capable of ensuring an improved fineness for a picture being displayed on the panel, without causing the above-mentioned problems such as a decrease in a displaying brightness and some misdischarges in discharge cells.

[0017] It is a second object of the present invention to provide an improved plasma display panel capable of preventing a reflection of an external light incident on the panel, thereby improving the contrast of a picture being displayed on the panel.

[0018] It is a third object of the present invention to

provide an improved plasma display panel capable having an improved resolution.

[0019] It is a fourth object of the present invention to provide an improved plasma display panel capable of preventing a warpage in partition walls (which are provided to divide a discharge space into a plurality of discharge cells), thereby preventing a possible deformation in the predetermined shape of the discharge cells.

[0020] It is a fifth object of the present invention to provide an improved plasma display panel capable of preventing the formation of unwanted slots between a front glass substrate and a rear glass substrate, thereby avoiding any possible defect caused by such slots in the display panel.

[0021] According to the present invention, there is provided a plasma display panel comprising: a front substrate; a plurality of row electrode pairs provided on the inner surface of the front substrate, said row electrode pairs being arranged in parallel with one another and extending in the row direction of the panel, with each row electrode pair forming a displaying line; a dielectric layer provided on the inner surface of the front substrate for covering the row electrode pairs; a rear substrate arranged in parallel with and space-apart from the front substrate, forming a discharge space therebetween; a plurality of column electrodes provided on the inner surface of the rear substrate, said column electrodes being arranged in parallel with one another and extending in the column direction of the panel, in a manner such that at each intersection of a row electrode pair with a column electrode there is formed a light emission unit; a partition wall assembly provided between the front substrate and the rear substrate, said partition wall assembly including a plurality of longitudinal partition walls and a plurality of lateral partition walls, thereby dividing the discharge space into a plurality of discharge cells. In particular, the dielectric layer has a plurality of projection portions located corresponding to and protruding toward the lateral partition walls of the partition wall assembly, in a manner such that there would be no slots formed between the dielectric layer and the lateral partition walls.

[0022] In one more aspect of the present invention, a slot is formed between the dielectric layer and each longitudinal partition wall of the partition wall assembly.

[0023] In one more aspect of the present invention, a fluorescent layer is formed to cover side faces of the longitudinal partition walls and the lateral partition walls and exposed portions of another dielectric layer formed on the inner surface of the rear substrate.

[0024] In one more aspect of the present invention, the partition wall assembly has a two-layer structure, one of which is a light absorbing layer located closer to the front substrate, and the other of which is a light reflecting layer located closer to the rear substrate.

[0025] In one more aspect of the present invention, each row electrode pair has two row electrodes each having a light absorbing layer facing the front substrate.

[0026] In one more aspect of the present invention,

each of the two row electrodes forming one electrode pair has a plurality of protruding portions, forming a plurality of discharge gaps between mutually facing protruding portions of the two row electrodes.

[0027] In one more aspect of the present invention, a mutual positional relationship between two row electrodes of a row electrode pair is alternatively changed from one displaying line to another, two mutually adjacent row electrodes of every two mutually adjacent displaying lines are connected to an identical common electrode main body.

[0028] In one more aspect of the present invention, protruding portions of two mutually adjacent row electrodes of every two mutually adjacent displaying lines are connected with each other.

[0029] In one more aspect of the present invention, there are formed a plurality of lateral light absorbing straps on the inner surface of the front substrate, with each lateral light absorbing strap being positioned between two mutually adjacent row electrodes of every two mutually adjacent displaying lines.

[0030] In one more aspect of the present invention, there are formed a plurality of longitudinal light absorbing straps on the inner surface of the front substrate, with each longitudinal light absorbing strap being positioned corresponding to one longitudinal partition wall.

[0031] In one more aspect of the present invention, a light absorbing layer is formed on the inner surface of the front substrate layer, said light absorbing layer having the same pattern corresponding to the lateral and longitudinal partition walls of the partition wall assembly.

[0032] In one more aspect of the present invention, protruding portions of two row electrodes forming one displaying line have mutually facing head portions which are inclined with respect to the row direction of the panel.

[0033] In one more aspect of the present invention, each displaying line includes a plurality of discharge cells repeatedly arranged in the order of R, G, B, each column includes a plurality of same color discharge cells, with every three discharge cells (R, G, B) arranged in a display line forming one picture element.

[0034] In one more aspect of the present invention, each displaying line includes a plurality of discharge cells repeatedly arranged in the order of R, G, B, one displaying line being deviated in the row direction from its adjacent displaying line by one discharge cell, with every three discharge cells (R, G, B) arranged in a display line forming one picture element.

[0035] In one more aspect of the present invention, each displaying line includes a plurality of discharge cells repeatedly arranged in the order of R, G, B, one displaying line being deviated in the row direction from its adjacent displaying line by half width of one discharge cell, with every three discharge cells (R, G, B) arranged in a display line forming one picture element.

[0036] In one more aspect of the present invention, each displaying line includes a plurality of discharge cells repeatedly arranged in the order of R, G, B, one

displaying line being deviated in the row direction from its adjacent displaying line by 1.5 times the width of one discharge cell, in a manner such that each pitch element may also be formed by three discharge cells (R, G, B) which together form a triangular configuration bridging over two mutually adjacent displaying lines.

[0037] In one more aspect of the present invention, each lateral partition wall of the partition wall assembly is divided into two portions by an elongated slot extending in the row direction of the panel.

[0038] In one more aspect of the present invention, each divided portion of each lateral partition wall has substantially the same width as that of each longitudinal partition wall of the partition wall assembly.

[0039] In one more aspect of the present invention, a plurality of light absorbing straps are formed on the inner surface of the front substrate, in positions corresponding to the elongated slots.

[0040] In one more aspect of the present invention, a plurality of light absorbing straps are formed on the inner surface of the front substrate, in positions corresponding to the longitudinal partition walls of the partition wall assembly.

[0041] In one more aspect of the present invention, at least the longitudinal partition walls of the partition wall assembly have a two-layer structure, one of which is a light absorbing layer facing toward the front substrate, and the other of which is a light reflecting layer facing toward the rear substrate.

[0042] In one more aspect of the present invention, each of two row electrodes of a row electrode pair includes an elongated main body portion extending in the row direction of the panel and a plurality of protruding portions extending in the column direction of the panel, so that a plurality of discharge gaps are formed between mutually facing protruding portions of two elongated main body portions. In particular, each elongated main body portion is made by a metal film. Further, each protruding portion is formed by a transparent electrically conductive film, with its base end connected to an elongated main body portion.

[0043] In one more aspect of the present invention, a light absorbing layer is formed on each elongated main body portion so that said light absorbing layer is interposed between the inner surface of the front substrate and the elongated main body portion.

[0044] In one more aspect of the present invention, one elongated main body portion is shared by two mutually adjacent row electrodes of two mutually adjacent displaying lines.

[0045] In one more aspect of the present invention, the outermost corner portions of each lateral partition wall are removed so as to form inclined surfaces thereon.

[0046] In one more aspect of the present invention, outer end portions of partition wall assembly are formed in positions not facing the projection portions of the dielectric layer.

[0047] In one more aspect of the present invention, outer end portions of each pair of lateral partition walls are combined with each other in positions not facing the projection portions of the dielectric layer.

5 [0048] In one more aspect of the present invention, the partition wall assembly is made of a light transmissible material.

10 [0049] In one more aspect of the present invention, each of two row electrodes of one row electrode pair has a plurality of protruding portions, thereby forming a plurality of discharge gaps between mutually facing protruding portions of the two row electrodes. Further, a mutual positional relationship between two row electrodes of one row electrode pair is alternatively changed from one displaying line to another. Moreover, one common electrode main body portion is shared by two mutually adjacent row electrodes of two mutually adjacent displaying lines.

15 [0050] The above objects and features of the present invention will become better understood from the following description with reference to the accompanying drawings.

BRIEF DESCRIPTION OF DRAWINGS

25 [0051] Fig. 1 is a plane view indicating a plasma display panel according to a first embodiment of the present invention.

[0052] Fig. 2 is a cross sectional view taken along a line VI-VI in Fig. 1.

30 [0053] Fig. 3 is a cross sectional view taken along a line V2-V2 in Fig. 1.

[0054] Fig. 4 is a cross sectional view taken along a line W1-W1 in Fig. 1.

35 [0055] Fig. 5 is a cross sectional view taken along a line W2-W2 in Fig. 1.

[0056] Fig. 6 is a plane view indicating a plasma display panel according to a second embodiment of the present invention.

40 [0057] Fig. 7 is a plane view indicating a plasma display panel according to a third embodiment of the present invention.

[0058] Fig. 8 is a plane view indicating a modified example of the third embodiment shown in Fig. 7.

45 [0059] Fig. 9 is a plane view indicating a plasma display panel according to a fourth embodiment of the present invention.

[0060] Fig. 10 is a cross sectional view taken along a line V3-V3 in Fig. 9.

50 [0061] Fig. 11 is a cross sectional view taken along a line V4-V4 in Fig. 9.

[0062] Fig. 12 is a cross sectional view taken along a line W3-W3 in Fig. 9.

55 [0063] Fig. 13 is a cross sectional view taken along a line W4-W4 in Fig. 9.

[0064] Fig. 14 is a plane view indicating a plasma display panel according to a fifth embodiment of the present invention.

[0065] Fig. 15 is a cross sectional view taken along a line V5-V5 in Fig. 14.

[0066] Fig. 16 is a cross sectional view taken along a line V6-V6 in Fig. 14.

[0067] Fig. 17 is a plane view indicating a plasma display panel according to a sixth embodiment of the present invention.

[0068] Fig. 18 is a plane view indicating a plasma display panel according to a seventh embodiment of the present invention.

[0069] Fig. 19 is a plane view indicating a plasma display panel according to an eighth embodiment of the present invention.

[0070] Fig. 20 is a plane view indicating a plasma display panel according to a ninth embodiment of the present invention.

[0071] Fig. 21 is a plane view indicating a plasma display panel according to a tenth embodiment of the present invention.

[0072] Fig. 22 is a plane view indicating a plasma display panel according to an eleventh embodiment of the present invention.

[0073] Fig. 23 is a cross sectional view taken along a line V7-V7 in Fig. 22.

[0074] Fig. 24 is a cross sectional view taken along a line V8-V8 in Fig. 22.

[0075] Fig. 25 is a cross sectional view taken along a line W5-W5 in Fig. 22.

[0076] Fig. 26 is a cross sectional view taken along a line W6-W6 in Fig. 22.

[0077] Fig. 27 is a plane view indicating a plasma display panel according to a twelfth embodiment of the present invention.

[0078] Fig. 28 is a cross sectional view taken along a line V9-V9 in Fig. 27.

[0079] Fig. 29 is a cross sectional view taken along a line V10-V10 in Fig. 27.

[0080] Fig. 30 is a plane view indicating a plasma display panel according to a thirteenth embodiment of the present invention.

[0081] Fig. 31 is a plane view indicating a plasma display panel according to a fourteenth embodiment of the present invention.

[0082] Fig. 32 is a plane view indicating a plasma display panel according to a fifteenth embodiment of the present invention.

[0083] Fig. 33 is a cross sectional view taken along a line V11-V11 in Fig. 32.

[0084] Fig. 34 is a cross sectional view taken along a line V12-V12 in Fig. 32.

[0085] Fig. 35 is a cross sectional view taken along a line W7-W7 in Fig. 32.

[0086] Fig. 36 is a cross sectional view taken along a line W8-W8 in Fig. 32.

[0087] Fig. 37 is a plane view indicating a plasma display panel according to a sixteenth embodiment of the present invention.

[0088] Fig. 38 is a plane view indicating a plasma display panel according to a seventeenth embodiment of the present invention.

play panel according to a seventeenth embodiment of the present invention.

[0089] Fig. 39 is a plane view indicating a plasma display panel according to an eighteenth embodiment of the present invention.

[0090] Fig. 40 is a plane view indicating a plasma display panel according to a nineteenth embodiment of the present invention.

[0091] Fig. 41 is a plane view indicating a plasma display panel according to a twentieth embodiment of the present invention.

[0092] Fig. 42 is a plane view indicating a plasma display panel showing the shape of modified partition wall assembly of the present invention.

[0093] Fig. 43 is a plane view indicating a plasma display panel according to a 21th embodiment of the present invention.

[0094] Fig. 44 is a cross sectional view taken along a line W9-W9 in Fig. 43.

[0095] Fig. 45 is a cross sectional view taken along a line W10-W10 in Fig. 43.

[0096] Fig. 46 is a cross sectional view taken along a line V13-V13 in Fig. 43.

[0097] Fig. 47 is a plane view indicating a plasma display panel according to a prior art.

[0098] Fig. 48 is a cross sectional view taken along a line V-V in Fig. 47.

[0099] Fig. 49 is a cross sectional view taken along a line W-W in Fig. 47.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENTS

First Embodiment

[0100] A first embodiment of the present invention is illustrated in Figs. 1 - 5.

[0101] Referring to Figs. 1 - 5, a surface discharge type AC-driven plasma display panel of the present invention has a front glass substrate 10 serving as a displaying surface for the panel, a plurality of row electrode pairs (X,Y) mutually parallelly disposed on the inner surface of the front glass substrate 10.

[0102] Each row electrode X includes a plurality of T-shaped transparent electrodes Xa consisting of a transparent electrically conductive film made of ITO, and an elongated bus electrode Xb consisting of a metal film which is connected with one end of each T-shaped transparent electrode Xa.

[0103] Similarly, each row electrode Y includes a plurality of T-shaped transparent electrodes Ya consisting of a transparent electrically conductive film made of ITO, and an elongated bus electrode Yb consisting of a metal film which is connected with one end of each T-shaped transparent electrode Ya.

[0104] Further, two row electrodes (X, Y) forming a row electrode pair are arranged in parallel to each other, with a plurality of discharge gaps g formed between the

T-shaped transparent electrodes Xa and the T-shaped transparent electrodes Ya, thereby forming one displaying line L for the plasma display panel (matrix display).

[0105] The T-shaped transparent electrodes Xa, Ya are formed on the inner surface of the front glass substrate 10 by vapor-depositing ITO thereon, followed by a patterning treatment with the use of a photolithographic method.

[0106] On the other hand, each elongated bus electrode Xb includes a black colour electrically conductive layer Xb' (facing the front glass substrate 10) and a main electrically conductive layer Xb". Similarly, each elongated bus electrode Yb includes a black colour electrically conductive layer Yb' (facing the front glass substrate 10) and a main electrically conductive layer Yb".

[0107] These bus electrodes Xb, Yb are formed by at first applying a silver paste (in which a black pigment has been mixed) to the inner surface of the front glass substrate 10, followed by a drying treatment, thereby obtaining a dried black color paste layer. Further, a silver paste is applied to the dried black color paste layer, followed by a patterning treatment with the use of a photolithographic method, and further through a sintering treatment, thus forming the bus electrodes Xb, Yb on the inner surface of the front glass substrate 10.

[0108] Further, a dielectric layer 11 is formed on the inner surface of the front glass substrate 10 in a manner such that it covers up all the row electrode pairs (X, Y). Moreover, the dielectric layer 11 includes a plurality of projection portions 11A located in positions corresponding to every two mutually adjacent bus electrodes Xb, Yb.

[0109] The dielectric layer 11 may be formed by at first preparing an amount of low melting point glass paste and then forming the paste into several layers of films each having a predetermined thickness, followed by laminating the films and a sintering treatment. The projection portions 11A may be formed by screen-printing (with a predetermined thickness) a similar low melting point glass paste on to the dielectric layer 11, followed by a similar sintering treatment.

[0110] Then, a protection layer 12 consisting of MgO is formed on the dielectric layer 11, thus covering the projection portions 11A.

[0111] On the other hand, the plasma display panel has a rear glass substrate 13 arranged in parallel with and space-apart from the front glass substrate 10. A plurality of column electrodes D are provided on the inner surface of the rear glass substrate 13, and arranged orthogonal to the row electrode pairs (X, Y), in positions corresponding to the T-shaped transparent electrodes Xa, Ya.

[0112] The column electrodes D are formed by vapor-depositing an Al alloy (such as Al-Mn alloy) on to the inner surface of the rear glass substrate 13, followed by a patterning treatment with the use of a photolithographic method.

[0113] Further, a white color dielectric layer 14 is

formed on the inner surface of the rear glass substrate 13 so as to cover up all the column electrodes D. Moreover, a plurality of mutually orthogonal partition walls 15a, 15b are formed on the dielectric layer 14, thus forming a #-like partition wall assembly 15, as shown in Figs. 1, 2 and 4.

[0114] The white color dielectric layer 14 may be formed by applying a glass paste (in which a white pigment has been mixed) to the inner surface of the rear glass substrate 13 and the column electrodes D, followed by a drying treatment.

[0115] The partition walls 15a are longitudinal partition walls arranged in the column direction of the panel, while the partition walls 15b are lateral partition walls arranged in the row direction of the panel and located in positions corresponding to the projection portions 11A of the dielectric layer 11.

[0116] By virtue of the #-like partition wall assembly 15, an electric discharge space formed between the front glass substrate 10 and the rear glass substrate 13 is divided into a plurality of smaller discharge spaces S (Fig. 1) each enclosing a pair of mutually facing T-shaped transparent electrodes Xa, Ya between a pair of row electrodes (X, Y).

[0117] In detail, each of the partition walls 15a and 15b has a two-layer structure including a black color layer (light absorbing layer) 15' (facing the front glass substrate 10) and a white color layer (light reflecting layer) 15" (facing the rear glass substrate 13).

[0118] The #-like partition wall assembly 15 may be formed in the following process. At first, a low melting point glass paste uniformly containing a white color pigment and a low melting point glass paste uniformly containing a black color pigment are applied successively to the dielectric layer 14, followed by a drying treatment. Then, a #-like mask is employed to selectively cut the thus formed white glass layer and the black glass layer by virtue of a sand blast treatment, thereby forming the desired #-like partition wall assembly 15.

[0119] As shown in Fig. 4, a gap r is formed between each longitudinal partition wall 15a and the protection layer 12. On the other hand, as shown in Fig. 2, there is not any gap formed between the lateral partition walls 15b and the protection layer 12.

[0120] A fluorescent layer 16 is formed in a manner such that it covers the side surfaces (facing the discharge spaces S) of the longitudinal partition walls 15a and the lateral partition walls 15b, further covers the exposed portions (facing the discharge spaces S) of the dielectric layer 14.

[0121] The fluorescent layer 16 is arranged such that its different color portions (R, G, B) are arranged repeatedly in the discharge spaces S in the row direction of the panel.

[0122] Then, a noble gas is sealed into the discharge spaces S.

[0123] In a plasma display panel constituted in the above manner, the row electrode pairs (X, Y) are used

to form displaying lines L for a matrix display, while the discharge spaces S formed by the #-like partition wall assembly 15 are used to form discharge cells C.

[0124] The operation of the plasma display panel made according to the present embodiment may be performed in the same manner as in the above-discussed prior art.

[0125] Namely, at first, an addressing operation is conducted so that an electric discharge is effected selectively among the discharge cells C between the row electrode pairs (X, Y) and the column electrodes D. As a result, a plurality of lit-up cells (discharge cells C where wall charges have been formed in the dielectric layer 11) and a plurality of extinguished cells (discharge cells C where wall charges are not formed in the dielectric layer 11) are distributed on the panel corresponding to a picture to be displayed.

[0126] Subsequently, discharge sustaining pulses are simultaneously applied to all the displaying lines L in a manner such that the row electrode pairs (X, Y) will alternatively receive the discharge sustaining pulses. In this manner, surface discharge phenomenon will occur in lit-up cells once the discharge sustaining pulses are applied.

[0127] At this moment, since ultraviolet light will be generated due to the surface discharge in the lit-up cells, the fluorescent layer 16 (R, G, B) will be excited to effect light emission, thereby displaying a picture on the plasma display panel.

[0128] In the plasma display panel of the present embodiment, since a fluorescent layer 16 is provided on the dielectric layer 14 to cover not only the exposed portions of the dielectric layer 14 but also all the side faces (facing the discharge spaces S) of the partition wall assembly 15, the surface area of the fluorescent layer 16, i.e., a light emission area within each discharge cell C has been increased, thus increasing the brightness of a picture being displayed on the panel.

[0129] At this time, even if the size of each discharge cell C is made smaller in order to increase a fineness and a clarity of a picture being displayed, it is still allowed to ensure a required brightness for a picture.

[0130] Further, as shown in Fig. 1, since the T-shaped transparent electrodes Xa, Ya of each row electrode pair (X, Y) are facing each other and are independently enclosed in discharge cells C (i.e., one discharge cell C contains one pair of transparent electrodes Xa, Ya), even if the size of each discharge cell C is made smaller in order to increase a fineness and a clarity of a picture being displayed, it is sure to prevent a discharge interference from one discharge cell to an adjacent discharge cell in the row direction of the panel (along each displaying line L).

[0131] Moreover, since the projection portions 11A are formed on the dielectric layer 11, and since the protection layer 12 covering the projection portions 11A are in tight contact with the lateral partition walls 15b, mutually adjacent discharge spaces S of mutually adjacent

cells C in the column direction of the panel are isolated from each other (Figs. 2 and 5). Therefore, it is also sure to prevent a discharge interference from one discharge cell to an adjacent discharge cell in the column direction of the panel.

[0132] On the other hand, as shown in Figs. 3 and 4, the upper surface of each longitudinal partition wall 15a is facing some areas (not having projections 11A) of the dielectric layer 11, forming a slot r between the upper surface of each longitudinal partition wall 15a and the protection layer 12. In this way, mutually adjacent discharge spaces S of mutually adjacent discharge cells C in the row direction of the panel (along each displaying line L) are connected with one another through the slots r, thereby producing a priming effect enabling a kind of chain discharge (discharging continuously from one cell to another), thus ensuring a stabilized discharge in the plasma display panel.

[0133] In addition, since the black color electrically conductive layers Xb', Yb' (facing the front glass substrate 10) are formed in the manner as shown in Figs. 2 and 3, it is sure to prevent a reflection of an external light coming from the outside through the front glass substrate 10, thereby enabling an improvement in the contrast of a picture being displayed on the plasma display panel.

[0134] Further, since the dielectric layer 14 formed on the inner surface of the rear glass substrate 13 is white in color, lights emitted by the fluorescent layer 16 are reflected towards the front glass substrate 10, thereby preventing the light from escaping towards the rear glass substrate 13, thus increasing the brightness of a picture being displayed on the panel.

[0135] Moreover, the dielectric layer 14 can also serve as a protection layer during a sand blast treatment.

[0136] In addition, since the black color layer 15' is formed on the partition assembly 15, it is further sure to prevent a reflection of an external light coming from the outside through the front glass substrate 10, thereby enabling a further improvement in the contrast of a picture being displayed on the plasma display panel.

[0137] Further, since the side faces of the partition wall assembly 15 are mainly formed by the white color layer 15'', lights emitted by the fluorescent layer 16 are reflected towards the front glass substrate 10, thus increasing the brightness of a picture being displayed on the panel.

Second Embodiment

[0138] A second embodiment of the present invention is illustrated in Fig. 6.

[0139] As shown in Fig. 6, a plasma display panel according to the second embodiment includes a plurality of displaying lines Li, Li+1 ..., along which there are disposed row electrodes (Xi, Yi) in accordance with an arrangement of (Yi, Xi), (Xi+1, Yi+1) ... in the column direction of the panel.

[0140] In this way, T-shaped transparent electrodes (X_{ai} , X_{ai+1}) of mutually adjacent row electrodes (X_i , X_{i+1}) are allowed to be connected to a common (elongated) bus electrode X_{bj} , thus enabling a total area occupied by the elongated bus electrodes to be smaller than that in the plasma display panel of the first embodiment (Figs. 1 - 5).

[0141] Further, each lateral wall 25b of a #-like partition wall assembly 25 is allowed to be narrower in its width than that in the plasma display panel of the first embodiment (Figs. 1 - 5), thus ensuring each discharge space S_1 to be larger than that in the first embodiment, thereby making it possible to increase a total surface area of a fluorescent layer within each discharge space S_1 , thus desirably increasing the brightness of the plasma display panel.

[0142] Moreover, with the use of the common (elongated) bus electrodes X_{bj} , it is allowed to reduce a discharge current during an electric discharge of the plasma display panel.

[0143] In addition, it is also possible that mutually adjacent T-shaped transparent electrodes (X_{ai} , X_{ai+1}) of mutually adjacent row electrodes (X_i , X_{i+1}) may be connected to each other at the end portions thereof.

Third Embodiment

[0144] A third embodiment of the present invention is illustrated in Fig. 7.

[0145] As shown in Fig. 7, a plasma display panel according to the third embodiment includes a plurality of displaying lines $Li-1'$, Li' , $Li+1'$..., along which there are disposed row electrodes (X_i' , Y_i'), in accordance with an arrangement of (Y_i-1' , X_i-1'), (X_i' , Y_i'), (Y_i+1' , X_i+1')... in the column direction of the panel.

[0146] In fact, T-shaped transparent electrodes (X_{ai-1}' , X_{ai}') of mutually adjacent row electrodes (X_{i-1}' , X_i') are allowed to be connected to a common (elongated) bus electrode X_{bj}' , transparent electrodes (Y_{ai}' , Y_{ai+1}') of mutually adjacent row electrodes (Y_i' , Y_{i+1}') are allowed to be connected to a common (elongated) bus electrode Y_{bj}' .

[0147] In this way, with respect to mutually adjacent displaying lines ($Li-1'$, Li'), mutually adjacent row electrodes (X_{i-1}' , X_i') are allowed to use a common bus electrode X_{bj}' . Similarly, with respect to mutually adjacent displaying lines (Li' , $Li+1'$), mutually adjacent row electrodes (Y_i' , Y_{i+1}') are allowed to use a common bus electrode Y_{bj}' . Such arrangement enables a total area occupied by elongated bus electrodes to be smaller than that in the plasma display panel of the second embodiment (Fig. 6).

[0148] Further, each lateral partition wall 25b' of a #-like partition wall assembly 25' is allowed to be narrower in its width than that in the plasma display panel of the first embodiment (Figs. 1 - 5), thus ensuring each discharge space S_1' to be larger than that in the first embodiment, thereby making it possible to increase a total

surface area of a fluorescent layer within each discharge space S_1' , thus desirably increasing the brightness of the plasma display panel.

[0149] Moreover, with the use of common bus electrodes X_{bj}' , Y_{bj}' , it is possible to reduce a discharge current during an electric discharge of the plasma display panel.

[0150] In addition, as shown in Fig. 8, it is possible that mutually adjacent T-shaped transparent electrodes (X_{ai-1}' , X_{ai}') of mutually adjacent row electrodes (X_{i-1}' , X_i') may be integrally connected to each other at the end portions thereof. Similarly, it is also possible that mutually adjacent T-shaped transparent electrodes (Y_{ai}' , X_{ai+1}') of mutually adjacent row electrodes (Y_i' , Y_{i+1}') may be integrally connected to each other at the end portions thereof.

Fourth Embodiment

[0151] A fourth embodiment of the present invention is illustrated in Figs. 9 - 13.

[0152] As shown in Figs. 9 - 13, a plasma display panel according to the fourth embodiment is almost the same as the plasma display panel of the first embodiment (Figs. 1 - 5) except the following differences.

[0153] Namely, the inner surface of the front glass substrate 10 has formed thereon a plurality of lateral light absorbing straps (light blocking straps) 30 and a plurality of longitudinal light absorbing straps (light blocking straps) 31. In detail, the lateral light absorbing straps 30 are so arranged that each of them is disposed between mutually adjacent (elongated) bus electrodes Y_b , X_b of mutually adjacent row electrodes (X , Y). On the other hand, longitudinal light absorbing straps 31 are so formed that each of them is facing a longitudinal partition wall 35a of a #-like partition wall assembly 35.

[0154] The #-like partition wall assembly 35 has a single-layer structure white in color, which is a difference between the fourth embodiment and the first embodiment.

[0155] In this way, all the portions on the inner surface of the front glass substrate 10 except those facing the discharge spaces S are covered up by the light absorbing straps 30, 31 and the black color electrically conductive layers X_b' , Y_b' (as in the first embodiment). Therefore, it is sure to prevent a reflection of an external light coming from outside through the front glass substrate 10, thereby enabling an improvement in the contrast of a picture being displayed on the plasma display panel.

[0156] Nevertheless, it is also allowed to provide only one sort of the two kinds of the light absorbing straps 30, 31, i.e., it is also possible to provide either the lateral straps 30 or the longitudinal straps 31.

[0157] Further, on the inner surface of the front glass substrate 10, there may be formed many pieces of different color filters (not shown) corresponding to different color portions (R, G, B) of the fluorescent layer 16 (located in the discharge spaces S).

[0158] At this time, the two kinds of the light absorbing straps 30, 31 may be located in positions corresponding to slots formed between the different color filters facing the discharge spaces S.

Fifth Embodiment

[0159] A fifth embodiment of the present invention is illustrated in Figs. 14 - 16.

[0160] As shown in Figs. 14 - 16, a plasma display panel according to the fifth embodiment is almost the same as the plasma display panel of the first embodiment (Figs. 1 - 5) except the following differences.

[0161] Namely, the inner surface of the front glass substrate 10 has formed thereon a #-like light absorbing layers 40 corresponding to the entire (all portions of) #-like partition wall assembly 45.

[0162] Bus electrodes Xob, Yob of row electrodes Xo, Yo are each formed by only one layer which is an electrically conductive layer, located under the light absorbing layers 40.

[0163] In this way, since the inner surface of the front glass substrate 10 is covered by the light absorbing layers 40 except the portions facing the discharge spaces S, it is sure to prevent a reflection of an external light coming from outside through the front glass substrate 10, thereby enabling an improvement in the contrast of a picture being displayed on the plasma display panel.

Sixth Embodiment

[0164] A sixth embodiment of the present invention is illustrated in Fig. 17.

[0165] As shown in Fig. 17, a plasma display panel according to the sixth embodiment has a partition wall assembly 55 including longitudinal partition walls 55a and lateral partition walls 55b.

[0166] In particular, each longitudinal partition wall 55a has a width h1 which is larger than that in any of the previous embodiments. Further, each end portion of each length (extending between two lateral partition walls 55b) of each longitudinal partition wall 55a becomes larger towards a lateral partition wall 55b.

[0167] Moreover, T-shaped transparent electrodes Xola, Yola of row electrodes Xo1, Yo1 have head portions Xo1a', Yo1a' which are inclined with respect to the displaying lines L and are facing each other with gaps g' formed therebetween.

[0168] In this way, if each longitudinal partition wall 55a has a larger width, and if a black color layer is formed on the longitudinal partition wall 55a (in the same manner as in the first embodiment shown in Figs. 1 - 5), and further, if black color light blocking straps (or layers) are formed on the inner surface of the front glass substrate 10 in positions corresponding to the partition wall assembly 55 (in the same manner as in the fourth and fifth embodiments shown in Figs. 9 - 16), these black color layers (or straps) may be made larger in their ar-

eas, thereby making it more exact to prevent a reflection of an external light coming from outside.

[0169] Referring again to Fig. 17, each discharge gap g' has a length x which is required to be 200 - 250 microns in order to reduce a discharge starting voltage. If the length is longer than 250 microns or shorter than 200 microns, the discharge starting voltage will undesirably increase.

Seventh Embodiment

[0170] A seventh embodiment of the present invention is illustrated in Fig. 18.

[0171] Fig. 18 is a plane view schematically indicating how a plurality of picture elements are formed by virtue of a plurality of discharge cells C including three kinds of colors R, G, B.

[0172] As shown in Fig. 18, a plurality of discharge cells C are formed by virtue of a #-like partition wall assembly 15A. DA is used to represent column electrodes.

[0173] The discharge cells C are arranged in each displaying line L (row direction) in the order of R, G, B repeatedly, and in each column (column direction) there are arranged a plurality of discharge cells belonging to only one kind of color.

[0174] In fact, every three discharge cells C (R, G, B) arranged in a display line L will form one picture element GA. Thus, a plurality of picture elements GA are aligned in the column direction.

Eighth Embodiment

[0175] An eighth embodiment of the present invention is illustrated in Fig. 19.

[0176] Fig. 19 is also a plane view schematically indicating how a plurality of picture elements are formed by virtue of a plurality of discharge cells C including three kinds of colors R, G, B.

[0177] As shown in Fig. 19, a plurality of discharge cells C are formed by virtue of a #-like partition wall assembly 15B. DB is used to represent column electrodes.

[0178] The discharge cells C are arranged in each displaying line L (row direction) in the order of R, G, B repeatedly, but with one displaying line L being deviated from its adjacent displaying line L by one discharge cell C in the row direction (arranged in a manner shown in Fig. 19).

[0179] In fact, every three discharge cells C (R, G, B) arranged in a display line L will form one picture element GB. Thus, when viewed in the column direction, one picture element GB is deviated from its adjacent (in column direction) picture element GB by one discharge cell C in the row direction.

[0180] In this way, since one picture element GB is deviated (when viewed in the column direction) from its adjacent (in column direction) picture element GB by one discharge cell C in the row direction, it is possible

to improve the resolution of a picture being displayed on the panel.

Ninth Embodiment

[0181] A ninth embodiment of the present invention is illustrated in Fig. 20.

[0182] Fig. 20 is also a plane view schematically indicating how a plurality of picture elements are formed by virtue of a plurality of discharge cells C including three kinds of colors R, G, B.

[0183] As shown in Fig. 20, a plurality of discharge cells C are formed by virtue of a #-like partition wall assembly 15C. DC is used to represent column electrodes.

[0184] In particular, when viewed in the column direction, two mutually adjacent (in column direction) discharge cells C are deviated from each other by half width of one cell C in the row direction.

[0185] Accordingly, each of color portions R, G, B of one displaying line L is deviated from a corresponding color portion of an adjacent displaying line L by half width of one cell C in the row direction.

[0186] For this reason, the column electrodes DC are formed in a zigzag configuration as shown in Fig. 20, thereby permitting the formation of the arrangement of discharge cells C shown in Fig. 20.

[0187] In this manner, since each picture element GC consists of three discharge cells C (R, G, B) arranged in the row direction, each of color portions R, G, B of one picture element on one displaying line L is deviated (in the row direction) from a corresponding color portion of a corresponding picture element of an adjacent displaying line L by half width of one cell C, it is allowed to further improve the resolution of a picture being displayed on the panel.

Tenth Embodiment

[0188] A tenth embodiment of the present invention is illustrated in Fig. 21.

[0189] Fig. 21 is also a plane view schematically indicating how a plurality of picture elements are formed by virtue of a plurality of discharge cells C including three kinds of colors R, G, B.

[0190] As shown in Fig. 21, a plurality of discharge cells C are formed by virtue of a #-like partition wall assembly 15D. DD is used to represent column electrodes.

[0191] In particular, when viewed in the column direction, two mutually adjacent (in column direction) discharge cells C are deviated from each other by half width of one cell C in the row direction.

[0192] In more detail, each of color portions R, G, B of one displaying line L is deviated (in the row direction) from a corresponding color portion of an adjacent displaying line L by 1.5 times the width of one cell C.

[0193] Accordingly, similar to the ninth embodiment, the column electrodes DD are formed in a zigzag con-

figuration as shown in Fig. 21, thereby permitting the formation of the arrangement of discharge cells C shown in Fig. 21.

[0194] In this manner, as shown in Fig. 21, each pitch element GD may also be formed by three discharge cells (R, G, B) which together form a triangular configuration bridging over two mutually adjacent displaying lines L, thereby further improving the resolution of a picture being displayed on the panel.

Eleventh Embodiment

[0195] An eleventh embodiment of the present invention is illustrated in Figs. 22 - 26.

[0196] Referring to Figs. 22 - 26, a surface discharge type AC-driven plasma display panel according to the eleventh embodiment of the present invention has a front glass substrate 10 serving as a displaying surface for the panel, a plurality of row electrode pairs (X, Y) parallelly disposed on the inner surface of the front glass substrate 10.

[0197] Each row electrode X includes a plurality of T-shaped transparent electrodes Xa each consisting of a transparent electrically conductive film made of ITO, and an elongated bus electrode Xb consisting of a metal film which is connected with one end of each T-shaped transparent electrode Xa.

[0198] Similarly, each row electrode Y includes a plurality of T-shaped transparent electrodes Ya each consisting of a transparent electrically conductive film made of ITO, and an elongated bus electrode Yb consisting of a metal film which is connected with one end of each T-shaped transparent electrode Ya.

[0199] Further, two row electrodes (X, Y) forming each row electrode pair are arranged in parallel to each other, with a plurality of discharge gaps g formed between the T-shaped transparent electrodes Xa, Ya, thereby forming one displaying line L for the display panel (matrix display).

[0200] The T-shaped transparent electrodes Xa, Ya are formed on the inner surface of the front glass substrate 10 by vapor-depositing ITO thereon, followed by a patterning treatment with the use of a photolithographic method.

[0201] On the other hand, each elongated bus electrode Xb includes a black colour electrically conductive layer Xb' (facing the front glass substrate 10) and a main electrically conductive layer Xb". Similarly, each elongated bus electrode Yb includes a black colour electrically conductive layer Yb' (facing the front glass substrate 10) and a main electrically conductive layer Yb".

[0202] The elongated bus electrodes Xb, Yb are formed by at first applying a silver paste (in which a black pigment has been mixed) to the inner surface of the front glass substrate 10, followed by a drying treatment, thereby obtaining a dried black color paste layer. Further, a silver paste is applied to the dried black color paste layer, followed by a patterning treatment with the

use of a photolithographic method, and further through a sintering treatment, thus forming the bus electrodes Xb, Yb on the inner surface of the front glass substrate 10.

[0203] Further, the inner surface of the front glass substrate 10 has formed thereon a plurality of lateral light absorbing straps (light blocking straps) 60 and a plurality of longitudinal light absorbing straps (light blocking straps) 61. In detail, the lateral light absorbing straps 60 are so arranged that each of them is disposed between mutually adjacent (elongated) bus electrodes Yb, Xb of mutually adjacent row electrodes (X, Y). On the other hand, longitudinal light absorbing straps 61 are so formed that each of them is facing a longitudinal partition wall 65a of a partition wall assembly 65.

[0204] Further, a dielectric layer 11 is formed on the inner surface of the front glass substrate 10 in a manner such that it covers up all the row electrode pairs (X, Y). Moreover, the dielectric layer 11 includes a plurality of projection portions 11A located in positions corresponding to every two adjacent bus electrodes Xb, Yb.

[0205] The dielectric layer 11 may be formed by at first preparing an amount of low melting point glass paste and then forming the paste into several layers of films each having a predetermined thickness, followed by laminating the films and a sintering treatment. The projection portions 11A may be formed by screen-printing (with a predetermined thickness) a similar low melting point glass paste on to the dielectric layer 11, followed by a similar sintering treatment.

[0206] Then, a protection layer 12 consisting of MgO is formed on the dielectric layer 11.

[0207] Similarly, the plasma display panel has a rear glass substrate 13 arranged in parallel with and space-apart from the front glass substrate 10. A plurality of column electrodes D are provided on the inner surface of the rear glass substrate 13, and arranged orthogonal to the row electrode pairs (X, Y), in positions corresponding to the T-shaped transparent electrodes Xa, Ya.

[0208] The column electrodes D are formed by vapor-depositing an Al alloy (such as Al-Mn alloy) on the inner surface of the rear glass substrate 13, followed by a patterning treatment with the use of a photolithographic method.

[0209] Further, a white color dielectric layer 14 is formed on the inner surface of the rear glass substrate 13 so as to cover up all the column electrodes D, and a plurality of mutually orthogonal partition walls 65a, 65b are formed on the dielectric layer 14, thereby forming a desired partition wall assembly 65.

[0210] The white color dielectric layer 14 may be formed by applying a glass paste (in which a white pigment has been mixed) to the inner surface of the rear glass substrate 13 and the column electrodes D, followed by a drying treatment.

[0211] The longitudinal partition walls 65a are arranged in the column direction of the panel, while the lateral partition walls 65b are arranged in the row direc-

tion of the panel corresponding to the projection portions 11A of the dielectric layer 11.

[0212] By virtue of the partition wall assembly 65, an electric discharge space formed between the front glass substrate 10 and the rear glass substrate 13 is divided into a plurality of smaller discharge spaces S (Fig. 22) each enclosing a pair of T-shaped transparent electrodes Xa, Ya between a pair of row electrodes (X, Y).

[0213] The partition wall assembly 65 may be formed in the following process. At first, a low melting point glass paste uniformly containing white color pigment is applied to the dielectric layer 14, followed by a drying treatment so as to form a white glass layer. Then, a ladder-like mask is employed to selectively cut the white glass layer with the use of a sand blast treatment, thereby forming a desired partition wall assembly 65 (including several ladder-like structures).

[0214] As shown in Fig. 25, a gap r is formed between each longitudinal partition wall 65a and the protection layer 12. On the other hand, as shown in Fig. 23, there is no any gap formed between the lateral partition walls 65b and the protection layer 12.

[0215] A fluorescent layer 16 is formed in a manner such that it covers the side surfaces (facing the discharge spaces S) of the longitudinal partition walls 65a and the lateral partition walls 65b, further covers the exposed portions (facing the discharge spaces S) of the dielectric layer 14.

[0216] However, the colors of the fluorescent layer 16 are so arranged that R, G, B are arranged repeatedly in the discharge spaces S in the row direction of the panel.

[0217] Then, a noble gas is sealed into the discharge spaces S.

[0218] In fact, as shown in Figs. 22 - 24, each lateral partition wall 65b has been divided into two portions 65b', 65b' separated from each other and an elongated slot SL is formed therebetween. Particularly, each elongated slot SL is located corresponding to a light absorbing strap 60 formed between two mutually adjacent displaying lines L on the inner surface of the front glass substrate 10.

[0219] Namely, the partition assembly 65 is formed into a plurality of ladder-like structures each extending in the row direction of the panel. Thus, a plurality of ladder-like structures are in parallel with one another, with an elongated slot SL formed between every two mutually adjacent ladder-like structures.

[0220] However, the width of each elongated slot SL is set in a manner such that each of the divided portions 65b', 65b' of each lateral partition wall 65b has the same width as that of each longitudinal partition wall 65a.

[0221] In a plasma display panel constituted in the above manner, the row electrode pairs (X, Y) are used to form displaying lines L for a matrix display, while the discharge spaces S formed by the ladder-like partition wall assembly 65 are used to serve as discharge cells C.

[0222] The operation of the plasma display panel made according to the present embodiment may be per-

formed in the same manner as in the above-discussed prior art.

[0223] Namely, at first, an addressing operation is conducted so that an electric discharge is effected selectively among the discharge cells C between the row electrode pairs (X, Y) and the column electrodes D. As a result, a plurality of lit-up cells (discharge cells C where wall charges have been formed in the dielectric layer 11) and a plurality of extinguished cells (discharge cells C where wall charges are not formed in the dielectric layer 11) are distributed on the panel corresponding to a picture to be displayed.

[0224] Subsequently, discharge sustaining pulses are simultaneously applied to all the displaying lines L in a manner such that the row electrode pairs (X, Y) will alternatively receive the discharge sustaining pulses. In this manner, surface discharge phenomenon will occur in lit-up cells once the discharge sustaining pulses are applied thereto.

[0225] At this moment, since ultraviolet light will be generated due to the surface discharge in the lit-up cells, the fluorescent layer 16 (R, G, B) will be excited to effect light emission, thereby displaying a picture on the plasma display panel.

[0226] In this way, since each lateral partition wall 65b is divided into two portions 65b', 65b' separated from each other by an elongated slot SL formed therebetween, and since the width of each elongated slot SL is set in a manner such that each of the divided portions 65b', 65b' of each lateral partition wall 65b has the same width as that of each longitudinal partition wall 65a, it is sure to prevent any troubles possibly caused by an expansion of the partition wall assembly 65 during a sintering treatment, therefore preventing warpage of the front glass substrate 10 or the rear glass substrate 13 so as to prevent deformation of the discharge cells C.

[0227] In this way, all the portions on the inner surface of the front glass substrate 10 except those facing the discharge spaces S are covered up by the light absorbing straps 60, 61 and the black color electrically conductive layers Xb', Yb' (as in the first embodiment). Therefore, it is sure to prevent a reflection of an external light coming from outside through the front glass substrate 10, thereby improving the contrast of a picture being displayed on the plasma display panel.

[0228] Nevertheless, it is also allowed to provide only one sort of the two kinds of the light absorbing straps 60, 61, i.e., it is also possible to provide either the lateral straps 60 or the longitudinal straps 61.

[0229] Further, on the inner surface of the front substrate 10, there may be formed many pieces of different color filters (not shown) corresponding to different color portions (R, G, B) of the fluorescent layer 16 (located in the discharge spaces S).

[0230] At this time, the two kinds of the light absorbing straps 60, 61 may be located in positions corresponding to slots formed between the different color filters facing the discharge spaces S.

Twelfth Embodiment

[0231] A twelfth embodiment of the present invention is illustrated in Figs. 27 - 29.

[0232] As shown in Figs. 27 - 29, a plasma display panel according to the twelfth embodiment has a plurality of row electrodes (Xo, Yo) arranged on the inner surface of the front glass substrate 10 in the same manner as in the above Eleventh embodiment.

[0233] Further, on the inner surface of the front glass substrate 10 there are provided a plurality of black color light absorbing straps (light blocking strap) 70 corresponding to longitudinal partition walls 65a and lateral partition walls 65b of a ladder-like partition wall assembly 65 and slots SL.

[0234] As shown in Fig. 28, elongated bus electrodes (Xob, Yob) of each row electrode pair (Xo, Yo) are each formed only of a main electrically conductive layer, and are located under the black color light absorbing straps 70.

[0235] Similar to the above eleventh embodiment, each lateral partition wall 65b has been divided into two portions 65b', 65' separated from each other and an elongated slot SL is formed therebetween.

[0236] Particularly, each elongated slot SL is located corresponding to a light absorbing strap 70 formed between two mutually adjacent displaying lines L on the inner surface of the front glass substrate 10.

[0237] However, the width of each elongated slot SL is set in a manner such that each of the divided portions 65b', 65b' of each lateral partition wall 65b has the same width as that of each longitudinal partition wall 65a.

[0238] In this way, since each of the divided portions 65b', 65b' of each lateral partition wall 65b has the same width as that of each longitudinal partition wall 65a, it is sure to prevent any troubles possibly caused by an expansion of the partition wall assembly 65 during a sintering treatment, therefore preventing warpage of the front glass substrate 10 or the rear glass substrate 13, so as to prevent deformation of the discharge cells.

[0239] Further, in this way, the inner surface of the front glass substrate 10 except those facing the discharge spaces S are covered up by the light absorbing straps 70. Therefore, it is sure to prevent a reflection of an external light coming from outside through the front glass substrate 10, thereby improving the contrast of a picture being displayed on the plasma display panel.

Thirteenth Embodiment

[0240] A thirteenth embodiment of the present invention is illustrated in Fig. 30.

[0241] As shown in Fig. 30, a plasma display panel according to the thirteenth embodiment includes a plurality of displaying lines Li-1', Li', Li+1' ..., along which there are disposed row electrodes in accordance with an arrangement of (Yi-1', Xi-1'), (Xi', Yi'), (Yi+1', Xi+1')... in the column direction of the panel.

[0242] In fact, T-shaped transparent electrodes (Xai-1', Xai') of mutually adjacent row electrodes (Xi-1', Xi') are integrally connected to each other at base portions thereof. Similarly, T-shaped transparent electrodes (Yai', Yai+i') of mutually adjacent row electrodes (Y1', Y+1') are integrally connected to each other at base portions thereof.

[0243] Further, the T-shaped transparent electrodes (Xai-1', Xai') of mutually adjacent row electrodes (Xi-1', Xi') are connected to a common (elongated) bus electrode Xbj', while the T-shaped transparent electrodes (Yai', Yai+i') of mutually adjacent row electrodes (Y1', Y+1') are connected to a common (elongated) bus electrode Ybj'.

[0244] Similar to the above eleventh and twelfth embodiments, each lateral partition wall 65b has been divided into two portions 65b', 65b' separated from each other and an elongated slot SL is formed therebetween.

[0245] Also, similar to the above eleventh and twelfth embodiments, the width of each elongated slot SL is set in a manner such that each of the divided portions 65b', 65' of each lateral partition wall 65b has the same width as that of each longitudinal partition wall 65a.

[0246] In this way, since each of the divided portions 65b', 65b' of each lateral partition wall 65b has the same width as that of each longitudinal partition wall 65a, it is sure to prevent any troubles possibly caused by an expansion of the partition assembly 65 during a sintering treatment therefore preventing warpage of the front glass substrate 10 or the rear glass substrate 13, so as to prevent deformation of the discharge cells.

[0247] Further, since the T-shaped transparent electrodes (Xai-1', Xai') of mutually adjacent row electrodes (Xi-1', Xi') are allowed to use a common (elongated) bus electrode Xbj', and since the T-shaped transparent electrodes (Yai', Yai+i') of mutually adjacent row electrodes (Y1', Y+1') are allowed to use a common (elongated) bus electrode Ybj', the areas occupied by the elongated bus electrodes Xbj' and Ybj' are allowed to be smaller than those occupied by the elongated bus electrodes in the eleventh embodiment shown in Figs. 22 - 26.

[0248] In this way, each lateral wall 65b of the partition wall assembly 65 is allowed to be narrower in its width than that in the plasma display panel of the eleventh embodiment (Figs. 22 - 26), thus ensuring each discharge space Si' to be larger than that in the eleventh embodiment, thereby making it possible to increase total surface area of the fluorescent layer within the discharge spaces S1', thus desirably increasing the brightness of the plasma display panel.

[0249] Moreover, with the use of common (elongated) bus electrodes Xbj', Ybj' it is possible to reduce a discharge current during an electric discharge of the plasma display panel.

[0250] Here, each of the (elongated) bus electrodes Xbj', Ybj' may be formed into a two-layer structure including a black color electrically conductive layer and a main electrically conductive layer. Alternatively, each of

the bus electrodes Xbj', Ybj' may be formed into a one-layer structure, while black color light absorbing straps may be interposed between the one-layer bus electrodes Xbj', Ybj' and the inner surface of the front glass substrate 10. In this way, it is sure to prevent a reflection of an external light coming from outside through the front glass substrate 10, thereby improving the contrast of a picture being displayed on the plasma display panel.

10 Fourteenth Embodiment

[0251] A fourteenth embodiment of the present invention is illustrated in Fig. 31.

[0252] As shown in Fig. 31, a plasma display panel according to the fourteenth embodiment includes a plurality of displaying lines Li, Li+1 ..., along which there are disposed row electrodes in accordance with an arrangement (Xi, Yi), (Yi+1, Xi+1) ... in the column direction of the panel.

[0253] Further, T-shaped transparent electrodes (Xai, Xai+1) of mutually adjacent row electrodes (Xi, Xi+1) are connected to a common (elongated) bus electrode Xbj.

[0254] Similar to the above eleventh to thirteenth embodiments, each of lateral partition walls 75b1, 75b2 ... of a partition wall assembly 75 is divided into two portions (75b1', 75b1'), (75b2', 75b2') separated from each other and elongated slots SL1, SL2 ... are formed therebetween.

[0255] Also, similar to the above eleventh to thirteenth embodiments, the width of each of the elongated slots SL1, SL2 ... is set in a manner such that each of the divided portions 75b1', 75b2' ... of the lateral partition walls 75b1, 75b2 ... has substantially the same width as that of each longitudinal partition wall 75a.

[0256] In this way, since the divided portions 75b1', 75b2' ... of the lateral partition walls 75b1, 75b2 ... of the partition wall assembly 75 have substantially the same width as that of each longitudinal partition wall 75a, it is sure to prevent any troubles possibly caused by an expansion of the partition wall assembly 75 during a sintering treatment, therefore preventing warpage of the front glass substrate 10 or the rear glass substrate 13 and a possible damage of the partition wall assembly 75, thereby preventing a deformation of the discharge cells.

[0257] Further, since mutually adjacent row electrodes (Xi, Xi+1) are allowed to use common (elongated) bus electrodes Xbj, the area occupied by the bus electrodes Xbj is allowed to be smaller than that occupied by the bus electrodes in the eleventh embodiment shown in Figs. 22 - 26.

[0258] In this way, lateral walls 75b1, 75b2 ... of the partition wall assembly 75 are allowed to be narrower in their width than those in the plasma display panel of the eleventh embodiment (Figs. 22 - 26), thus ensuring each discharge space Si' to be larger than that in the eleventh embodiment, thereby making it possible to increase total surface area of the fluorescent layer within

the discharge spaces S1', thus desirably increasing the brightness of the plasma display panel.

[0259] Moreover, with the use of each common (elongated) bus electrode Xbj, it is possible to reduce a discharge current during an electric discharge of the plasma display panel.

Fifteenth Embodiment

[0260] A fifteenth embodiment of the present invention is illustrated in Figs. 32 - 36.

[0261] Referring to Figs. 32 - 36, a plasma display panel made according to the fifteenth embodiment has a front glass substrate 10 serving as a displaying surface for the panel, a plurality of row electrode pairs (X, Y) parallelly disposed on the inner surface of the front glass substrate 10.

[0262] Each row electrode X includes a plurality of T-shaped transparent electrodes Xa each consisting of a transparent electrically conductive film made of ITO, and an elongated bus electrode Xb consisting of a metal film which is connected with one end of each T-shaped transparent electrode Xa.

[0263] Similarly, each row electrode Y includes a plurality of T-shaped transparent electrodes Ya each consisting of a transparent electrically conductive film made of ITO, and an elongated bus electrode Yb consisting of a metal film which is connected with one end of each T-shaped transparent electrode Ya.

[0264] Further, two row electrodes (X, Y) forming a row electrode pair are arranged in parallel to each other, with a plurality of discharge gaps g formed between the T-shaped transparent electrodes Xa and the T-shaped transparent electrodes Ya, thereby forming one displaying line L for the display panel (matrix display).

[0265] The T-shaped transparent electrodes Xa, Ya are formed on the inner surface of the front glass substrate 10 by vapor-depositing ITO thereon, followed by a patterning treatment with the use of a photolithographic method.

[0266] On the other hand, each elongated bus electrode Xb includes a black colour electrically conductive layer Xb' (facing the front glass substrate 10) and a main electrically conductive layer Xb". Similarly, each elongated bus electrode Yb includes a black colour electrically conductive layer Yb' (facing the front glass substrate 10) and a main electrically conductive layer Yb".

[0267] The elongated bus electrodes Xb, Yb are formed by at first applying a silver paste (in which a black pigment has been mixed) to the inner surface of the front glass substrate 10, followed by a drying treatment, thereby obtaining a dried black color paste layer. Further, a silver paste is applied to the dried black color paste layer, followed by a patterning treatment with the use of a photolithographic method, and further through a sintering treatment, thus forming the elongated bus electrodes Xb, Yb on the inner surface of the front glass substrate 10.

[0268] Further, the inner surface of the front glass substrate 10 has formed thereon a plurality of lateral light absorbing straps (light blocking straps) 80 and a plurality of longitudinal light absorbing straps (light blocking straps) 81. In detail, the lateral light absorbing straps 80 are so arranged that each of them is disposed between mutually adjacent elongated bus electrodes Yb, Xb of mutually adjacent row electrodes (X, Y). On the other hand, light absorbing straps 81 are so formed that each of them is facing a longitudinal partition wall 85a of a #-like partition wall assembly 85.

[0269] Further, a dielectric layer 11' is formed on the inner surface of the front glass substrate 10 in a manner such that it covers up all the row electrode pairs (X, Y).

[0270] The dielectric layer 11' may be formed by at first preparing an amount of low melting point glass paste and then forming the paste into several layers of films each having a predetermined thickness, followed by laminating the films and a sintering treatment.

[0271] Then, a protection layer 12' consisting of MgO is formed on the exposed surface of the dielectric layer 11'.

[0272] On the other hand, the plasma display panel has a rear glass substrate 13 arranged in parallel with and space-apart from the front glass substrate 10. A plurality of column electrodes D are provided on the inner surface of the rear glass substrate 13, and arranged orthogonal to the row electrode pairs (X, Y), in positions corresponding to the T-shaped transparent electrodes Xa, Ya.

[0273] The column electrodes D are formed by vapor-depositing an Al alloy (such as Al-Mn alloy) on the inner surface of the rear glass substrate 13, followed by a patterning treatment with the use of a photolithographic method.

[0274] Further, a white color dielectric layer 14 is formed on the inner surface of the rear glass substrate 13 so as to cover up all the column electrodes D, a plurality of mutually orthogonal partition walls 85a, 85b are formed on the dielectric layer 14.

[0275] The white color dielectric layer 14 may be formed by applying a glass paste (in which a white pigment has been mixed) to the inner surface of the rear glass substrate 13 and the column electrodes D, followed by a drying treatment.

[0276] The partition walls 85a are longitudinal partition walls arranged in the column direction of the panel corresponding to the column electrodes D, while the partition walls 85b are lateral partition walls arranged in the row direction of the panel, thereby forming a partition wall assembly 85 in contact with the surface of the protection layer 12'.

[0277] By virtue of the partition wall assembly 85, an electric discharge space formed between the front glass substrate 10 and the rear glass substrate 13 is divided into a plurality of smaller discharge spaces S (Fig. 32) each enclosing a pair of T-shaped transparent electrodes Xa, Ya between a pair of row electrodes (X, Y).

[0278] Then, as shown in Fig. 32, a plurality of slits S1 are formed on the longitudinal partition walls 85a so that every two adjacent discharge spaces S are communicated with each other.

[0279] In addition, as shown in Figs. 32 - 34, each lateral partition wall 85b has been divided into two portions 85b', 85b' separated from each other and an elongated slot SL is formed therebetween. Particularly, each elongated slot SL is located corresponding to a light absorbing strap 80 formed between two mutually adjacent displaying lines L on the inner surface of the front glass substrate 10.

[0280] However, the width of each elongated slot SL is set in a manner such that each of the divided portions 85b', 85b' of each lateral partition wall 85b has the same width as that of each longitudinal partition wall 85a.

[0281] The partition assembly 85 may be formed in the following process. At first, a low melting point glass paste uniformly containing a white color pigment is applied to the dielectric layer 14, followed by a drying treatment. Then, a specifically shaped mask is employed to selectively cut the white glass layer with the use of a sand blast treatment, thereby forming the desired partition wall assembly 85.

[0282] A fluorescent layer 16 is formed in a manner such that it covers the side surfaces (facing the discharge spaces S) of the longitudinal partition walls 85a and the lateral partition walls 85b, further covers the exposed portions (facing the discharge spaces S) of the dielectric layer 14.

[0283] However, the colors of the fluorescent layer 16 are so arranged that R, G, B are arranged repeatedly in the discharge spaces S in the row direction of the panel (as shown in Fig. 35).

[0284] Then, a noble gas is sealed into the discharge spaces S. In a plasma display panel constituted in the above manner, the row electrode pairs (X,Y) are used to form displaying lines L for a matrix display, while the discharge spaces S formed by partition wall assembly 85 are used to serve as discharge cells C.

[0285] The operation of the plasma display panel made according to the present embodiment may be performed in the same manner as in the previous embodiments.

[0286] Namely, at first, an addressing operation is conducted so that an electric discharge is effected selectively among the discharge cells C between the row electrode pairs (X, Y) and the column electrodes D. As a result, a plurality of lit-up cells (discharge cells C where wall charges have been formed in the dielectric layer 11') and a plurality of extinguished cells (discharge cells C where wall charges are not formed in the dielectric layer 11') are distributed on the panel corresponding to a picture to be displayed.

[0287] Subsequently, discharge sustaining pulses are simultaneously applied to all the displaying lines L in a manner such that the row electrode pairs (X, Y) will alternatively receive the discharge sustaining pulses. In

this manner, surface discharge phenomenon will occur in lit-up cells once the discharge sustaining pulses are applied thereto.

[0288] At this moment, since ultraviolet light will be generated due to the surface discharge in the lit-up cells, the fluorescent layer 16 (R, G, B) will be excited to effect light emission, thereby displaying a picture on the plasma display panel.

[0289] In use of the plasma display panel, although the upper surface of the partition wall assembly 85 is in tight contact with the inner surface of the protection layer 12', a plurality of slits S1 are formed on the longitudinal partition walls 85a so that every two adjacent discharge spaces S are communicated with each other. In this way, the discharging gas and priming particles sealed in one discharge space S is allowed to move to its adjacent discharge space S, thereby producing a priming effect enabling a kind of chain discharge (discharging continuously from one cell to another), thus ensuring a stabilized discharge in the plasma display panel.

[0290] Further, since each lateral partition wall 85b is divided into two portions 85b', 85b' separated from each other by an elongated slot SL formed therebetween, and since the width of each elongated slot SL is set in a manner such that each of the divided portions 85b', 85b' of each lateral partition wall 85b has the same width as that of each longitudinal partition wall 85a, it is sure to prevent any troubles possibly caused by an expansion of the partition wall assembly 85 during a sintering treatment, therefore preventing warpage of the front glass substrate 10 or the rear glass substrate 13, so as to prevent deformation of the discharge cells.

Sixteenth Embodiment

[0291] A sixteenth embodiment of the present invention is illustrated in Fig. 37.

[0292] Referring to Fig. 37, a plasma display panel made according to the sixteenth embodiment is almost the same as that described in the above fifteenth embodiment except that a plurality of slits sl' are formed on lateral partition walls 95b of a partition wall assembly 95 in positions not facing the T-shaped transparent electrodes Xa, Ya, in a manner such that every two discharge spaces S mutually adjacent to each other in the column direction of the panel are communicated with each other.

[0293] In this way, since a plurality of slits sl' are formed on lateral partition walls 95b of the partition wall assembly 95 in positions not facing the T-shaped transparent electrodes Xa, Ya, a possible spreading phenomenon of discharge may be prohibited by virtue of the lateral partition walls 95b of the partition wall assembly 95.

Seventeenth Embodiment

[0294] A seventeenth embodiment of the present invention is illustrated in Fig. 38.

[0295] Fig. 38 is a plane view schematically indicating how a plurality of picture elements GA are formed by virtue of a plurality of discharge cells C including three kinds of colors R, G, B.

[0296] As shown in Fig. 38, a plurality of discharge cells C are formed by virtue of a ladder-like partition wall assembly 15A. DA is used to represent column electrodes.

[0297] The discharge cells C are arranged in each displaying line L (row direction) in the order of R, G, B repeatedly, and in each column (column direction) there are arranged a plurality of discharge cells belonging to only one kind of color.

[0298] In fact, every three discharge cells C (R, G, B) arranged in a display line L will form one picture element GA. Thus, a plurality of picture elements GA are aligned in the column direction.

[0299] In this way, since each of lateral partition walls 15Ab of the partition assembly 15A is divided into two portions 15Ab', 15Ab', and since each divided portion 15Ab' has substantially the same widths as that of each longitudinal partition wall 15Aa, it is sure to prevent any troubles possibly caused by an expansion of the partition wall assembly 15A during a sintering treatment, therefore preventing warpage of the front glass substrate 10 or the rear glass substrate 13 and a possible damage of the partition wall assembly 15A, thereby preventing a deformation of the discharge cells.

Eighteenth Embodiment

[0300] An eighteenth embodiment of the present invention is illustrated in Fig. 39.

[0301] Fig. 39 is also a plane view schematically indicating how a plurality of picture elements GB are formed by virtue of a plurality of discharge cells C including three kinds of colors R, G, B.

[0302] As shown in Fig. 39, a plurality of discharge cells C are formed by virtue of a ladder-like partition assembly 15B. DB is used to represent column electrodes.

[0303] The discharge cells C are arranged in each displaying line L (row direction) in the order of R, G, B repeatedly, but with one displaying line L being deviated from its adjacent (in column direction) displaying line L by one discharge cell C in the row direction.

[0304] In fact, every three discharge cells C (R, G, B) arranged in a display line L will form one picture element GB. Thus, when viewed in the column direction, one picture element GB is deviated (in the row direction) from its adjacent (in column direction) picture element GB by one discharge cell C.

[0305] In this way, since one picture element GB is deviated (in row direction) from its adjacent (in column direction) picture element GB by one discharge cell C, it is possible to improve the resolution of a picture being displayed on the panel.

[0306] Further, since each of lateral partition walls 15Bb of the partition wall assembly 15B is divided into

two portions 15Bb', 15Bb', and since each divided portion 15Bb' has substantially the same width as that of each longitudinal partition wall 15Ba, it is sure to prevent any troubles possibly caused by an expansion of the partition wall assembly 15B during a sintering treatment, therefore preventing warpage of the front glass substrate 10 or the rear glass substrate 13 and a possible damage of the partition wall assembly 15B, thereby preventing a deformation of the discharge cells.

Nineteenth Embodiment

[0307] A nineteenth embodiment of the present invention is illustrated in Fig. 40.

[0308] Fig. 40 is also a plane view schematically indicating how a plurality of picture elements GC are formed by virtue of a plurality of discharge cells C including three kinds of colors R, G, B.

[0309] As shown in Fig. 40, a plurality of discharge cells C are formed by virtue of a ladder-like partition assembly 15C. DC is used to represent column electrodes.

[0310] In particular, when viewed in the column direction, two mutually adjacent (in column direction) discharge cells C are deviated from each other by half width of one cell C in the row direction.

[0311] Accordingly, each of color portions R, G, B of one displaying line L is deviated from a corresponding color portion of an adjacent displaying line L by half width of one cell C in the row direction.

[0312] For this reason, the column electrodes DC are formed in a zigzag configuration as shown in Fig. 40, thereby permitting the formation of the above arrangement of discharge cells C shown in Fig. 40.

[0313] In this manner, since each picture element GC consists of three discharge cells C (R, G, B) arranged in the row direction, each of color portions R, G, B of one picture element on one displaying line L is deviated (in the row direction) from a corresponding color portion of a corresponding picture element on an adjacent displaying line L by half width of one cell C, it is allowed to further improve the resolution of a picture being displayed on the panel.

[0314] Further, since each of lateral partition walls 15Cb of the partition wall assembly 15C is divided into two portions 15Cb', 15Cb', and since each divided portion 15Cb' has substantially the same width as that of each longitudinal partition wall 15Ca, it is sure to prevent any troubles possibly caused by an expansion of the partition wall assembly 15C during a sintering treatment, therefore preventing warpage of the front glass substrate 10 or the rear glass substrate 13 and a possible damage of the partition wall assembly 15C, thereby preventing a deformation of the discharge cells.

Twentieth Embodiment

[0315] A twentieth embodiment of the present invention is illustrated in Fig. 41.

[0316] Fig. 41 is also a plane view schematically indicating how a plurality of picture elements GD are formed by virtue of a plurality of discharge cells C including three kinds of colors R, G, B.

[0317] As shown in Fig. 41, a plurality of discharge cells C are formed by virtue of partition wall assembly 15D. DD is used to represent column electrodes.

[0318] In particular, when viewed in the column direction, two mutually adjacent (in column direction) discharge cells C are deviated from each other by half width of one cell C in the row direction.

[0319] In more detail, each of color portions R, G, B of one displaying line L is deviated (in the row direction) from a corresponding color portion of an adjacent displaying line L by 1.5 times the width of one cell C.

[0320] Accordingly, similar to the nineteenth embodiment, the column electrodes DD are formed in a zigzag configuration as shown in Fig. 41, thereby permitting the formation of the above arrangement of discharge cells C shown in Fig. 41.

[0321] In this manner, as shown in Fig. 41, each pitch element GD may also be formed by three discharge cells (R, G, B) which together form a triangular configuration bridging over two mutually adjacent displaying lines L, thereby further improving the resolution of a picture being displayed on the panel.

[0322] Further, since each of lateral partition walls 15Db of the partition wall assembly 15D is divided into two portions 15Db', 15Db', and since each divided portion 15Db' has substantially the same width as that of each longitudinal partition wall 15Da, it is sure to prevent any troubles possibly caused by an expansion of the partition wall assembly 15D during a sintering treatment, therefore preventing warpage of the front glass substrate 10 or the rear glass substrate 13 and a possible damage of the partition wall assembly 15D, thereby preventing a deformation of the discharge cells.

First Additional Embodiment

[0323] Fig. 42 is a plane view indicating a plurality of partition wall assemblies suitable for use in any plasma display panel of the embodiments shown in Figs. 22 - 41.

[0324] As shown in Fig. 42, each partition wall assembly 15A has a plurality of vertical partition walls 15Aa and two horizontal partition walls 15Ab, thereby forming a ladder-like configuration providing a plurality of discharge cells C.

[0325] In practice, a plurality of partition wall assemblies 15A are arranged in parallel to one another with a slot SL formed between every two mutually adjacent partition wall assemblies 15A, 15A. In this way, an entire discharge space formed between a front glass substrate 10 and a rear glass substrate 13 may be divided into a plurality of smaller discharge spaces by virtue of several partition wall assemblies 15A.

[0326] Further, the leftmost and rightmost discharge cells C' of each partition wall assembly 15A are set to

be dummy cells. The corner portions (on the outside of the dummy cells C') of each partition wall assembly 15A are removed so as to form inclined surfaces 15Ac.

[0327] By removal of the corner portions (on the outside of the dummy cells C') of each partition wall assembly 15A, it is sure to remove any undesired build-up of a material (for forming the partition wall assembly 15A) from these positions.

[0328] The reason for the removal of the build-up may be explained as follows.

[0329] If any build-up of a material (for forming the partition wall assembly 15A) are not avoided, when the front glass substrate 10 and the rear glass substrate 13 are brought together to form a display panel, the two glass substrates will get in contact with the build-up portions of the partition wall assembly 15 while leaving the other portions thereof in a floating condition. Consequently, a vibration will happen on the substrates when the plasma display panel is being driven. Therefore, by removal of the corner portions (on the outside of the dummy cells C') of each partition wall assembly 15A, it is sure to remove any undesired build-up of a material (for forming the partition wall assembly 15A) from these positions, thereby ensuring that the two glass substrates will be in a uniform contact with the partition wall assembly 15A.

21th Embodiment

[0330] A 21th embodiment of the present invention is illustrated in Figs. 43 - 46.

[0331] As shown in Figs. 43 - 46, a plasma display panel according to the 21th embodiment has a partition wall assembly 105 including a plurality of longitudinal partition walls 105a and a plurality of lateral partition walls 105b. By virtue of the partition wall assembly 105, a discharge space formed between the front glass substrate 10 and the rear glass substrate 13 is divided into a plurality of discharge cells C.

[0332] On the inner surface of the front glass substrate 10, there are formed a plurality of row electrodes X each including a plurality of transparent electrodes Xa and an elongated bus electrode Xb, and a plurality of row electrodes Y each including a plurality of transparent electrodes Ya and an elongated bus electrode Yb, thereby forming a plurality of row electrode pairs (X, Y).

[0333] Further, a dielectric layer 11 is formed on the inner surface of the front glass substrate 10 in a manner such that the row electrodes (X, Y) are covered up by the dielectric layer 11. In particular, the dielectric layer 11 has a plurality of projection portions 11A located in positions corresponding to every two adjacent bus electrodes Xb, Yb.

[0334] Then, a protection layer 12 consisting of MgO is formed to cover the dielectric layer 11.

[0335] On the other hand, the plasma display panel has a rear glass substrate 13 arranged in parallel with and space-apart from the front glass substrate 10. A plu-

ality of column electrodes D are provided on the inner surface of the rear glass substrate 13, and arranged orthogonal to the row electrode pairs (X, Y), in positions corresponding to the transparent electrodes Xa, Ya.

[0336] Further, a white color dielectric layer 14 is formed on the inner surface of the rear glass substrate 13 so as to cover up all the column electrodes D, and a plurality of ladder-like partition wall assemblies 105 are formed on the dielectric layer 14, extending in the row direction of the plasma display panel.

[0337] Each ladder-like partition wall assembly 105 includes a plurality of short partition walls 105a (extending in the column direction of the panel), and a pair of long partition walls 105b (extending in the row direction of the panel) corresponding to the projection portions 11A of the dielectric layer 11, thereby forming a ladder-like partition wall assembly 105 (Fig. 43).

[0338] By virtue of the plurality of ladder-like partition wall assemblies 105, an electric discharge space formed between the front glass substrate 10 and the rear glass substrate 13 is divided into a plurality of discharge cells C each enclosing a pair of transparent electrodes Xa, Ya between a pair of row electrodes (X, Y).

[0339] In Fig. 43, Ca and Ca' are used to represent dummy cells not enclosing row electrodes (X, Y). These dummy cells Ca and Ca' are formed on the outer ends (right and left) of each ladder-like partition wall assembly 105 and are located on the outside of the displaying area of the plasma display panel.

[0340] Referring again to Fig. 43, outer portions of the two lateral partition walls 105b of each ladder-like partition wall assembly 105, located in the dummy cell Ca' outwardly of the dummy cell Ca which is positioned adjacent to a discharge cell C (located on the right side of line m in the figure, i.e., within the displaying area of the plasma display panel), are bent toward each other so as to form bent portions 105b' which are connected with each other at a position between two adjacent projection portions 11A of the dielectric layer 11.

[0341] In this way, a plurality of dummy cells Ca' each having a generally triangular shape are formed by virtue of the bent portions 105b' of the lateral partition walls 105b.

[0342] Although not shown in Fig. 43, the structure on the right side of the plasma display panel is just the same as that on the left side thereof.

[0343] With the use of the above structure, it is allowed to ensure that even if there is a possibility that undesired build-up β of a material (for forming the partition wall assembly) will occur (shown in Fig. 43) during a sintering treatment for the formation of the ladder-like partition wall assembly 105 (made of a glass), such kind of build-up β can only form in positions not facing the projection portions 11A of the dielectric layer 11.

[0344] In this way, as shown in Figs. 45 and 46, since the build-up β can only occur in slots s formed between the partition wall assembly 105 and the dielectric layer 11, when the front glass substrate 10 and the rear glass

substrate 13 are brought together to form the plasma display panel, it can be made sure that the build-up β will not get in contact with the projection portions 11A of the dielectric layer 11, thereby avoiding the formation of some unwanted slots between the lateral partition walls 105b of the partition wall assembly 105 and the projection portions 11A of the dielectric layer 11.

Second Additional Embodiment

[0345] Although it has been described in the above first embodiment (Figs. 1 - 5) that the partition wall assembly has a two-layer structure including a black color layer and a white color layer, it is also possible that such a partition wall assembly has a one-layer structure including only a white color layer. Further, the partition wall assembly may also be formed into a light-transmissible structure formed by a low melting point glass not containing any pigment.

[0346] By forming the light-transmissible partition wall assembly, a light generated in each discharge cell is allowed to be randomly reflected within the partition wall assembly so as to be widely spread on to the front glass substrate. Therefore, it is possible to improve an apparent numerical aperture so as to increase the brightness of the plasma display panel.

[0347] Further, it is also possible that a black color layer (light absorbing layer) may be formed on the upper surface of the light-transmissible partition wall assembly, thereby forming a two-layer structure including a black color layer (light absorbing layer) and a light-transmissible layer (transparent layer).

[0348] While the presently preferred embodiments of this invention have been shown and described above, it is to be understood that these disclosures are for the purpose of illustration and that various changes and modifications may be made without departing from the scope of the invention as set forth in the appended claims.

Claims

1. A plasma display panel comprising:

a front substrate (10);

a plurality of row electrode pairs (X, Y) provided on the inner surface of the front substrate (10), said row electrode pairs (X, Y) being arranged in parallel with one another and extending in the row direction of the panel, with each row electrode pair (X, Y) forming a displaying line (L);

a dielectric layer (11) provided on the inner surface of the front substrate (10) for covering the row electrode pairs (X, Y);

a rear substrate (13) arranged in parallel with and space-apart from the front substrate (10), forming a discharge space (S) therebetween;

a plurality of column electrodes (D) provided on the inner surface of the rear substrate (13), said column electrodes (D) being arranged in parallel with one another and extending in the column direction of the panel, in a manner such that at each intersection of a row electrode pair (X, Y) with a column electrode (D) there is formed a light emission unit;

a partition wall assembly (15) provided between the front substrate (10) and the rear substrate (13), said partition wall assembly (15) including a plurality of longitudinal partition walls (15a) and a plurality of lateral partition walls (15b), thereby dividing the discharge space (S) into a plurality of discharge cells (C);

wherein the dielectric layer (11) has a plurality of projection portions (11A) located corresponding to and protruding toward the lateral partition walls (15b) of the partition wall assembly (15), in a manner such that there would be no slots formed between the dielectric layer (11) and the lateral partition walls (15b).

2. The plasma display panel according to claim 1, wherein a slot (r) is formed between the dielectric layer (11) and each longitudinal partition wall (15a) of the partition wall assembly (15).
3. The plasma display panel according to claim 1, wherein a fluorescent layer (16) is formed to cover side faces of the longitudinal partition walls (15a) and the lateral partition walls (15b) and exposed portions of another dielectric layer (11) formed on the inner surface of the rear substrate (13).
4. The plasma display panel according to claim 1, wherein the partition wall assembly (15) has a two-layer structure, one of which is a light absorbing layer (15') located closer to the front substrate, and the other of which is a light reflecting layer (15'') located closer to the rear substrate (13).
5. The plasma display panel according to claim 1, wherein each row electrode pair (X, Y) has two row electrodes each having a light absorbing layer (15') facing the front substrate (10).
6. The plasma display panel according to claim 5, wherein each of the two row electrodes (X, Y) forming one electrode pair has a plurality of protruding portions (11A), forming a plurality of discharge gaps (g) between mutually facing protruding portions of

the two row electrodes (X, Y).

7. The plasma display panel according to claim 1, wherein a mutual positional relationship between two row electrodes (X, Y) of a row electrode pair is alternatively changed from one displaying line (L) to another, two mutually adjacent row electrodes (Xi, Xi+1, Yi, Yi+1) of every two mutually adjacent displaying lines (Li-1', Li') are connected to an identical common electrode main body (Xbj').
8. The plasma display panel according to claim 6, wherein protruding portions (11A) of two mutually adjacent row electrodes (Xi, Xi+1, Yi, Yi+1) of every two mutually adjacent displaying lines (Li-1', Li') are connected with each other.
9. The plasma display panel according to claim 1, wherein there are formed a plurality of lateral light absorbing straps (30) on the inner surface of the front substrate (10), with each lateral light absorbing strap (30) being positioned between two mutually adjacent row electrodes (Xi, Xi+1, Yi, Yi+1) of every two mutually adjacent displaying lines (Li-1', Li').
10. The plasma display panel according to claim 1, wherein there are formed a plurality of longitudinal light absorbing straps (31) on the inner surface of the front substrate (10), with each longitudinal light absorbing strap (31) being positioned corresponding to one longitudinal partition wall (35a).
11. The plasma display panel according to claim 1, wherein a light absorbing layer (40) is formed on the inner surface of the front substrate (10) layer, said light absorbing layer (40) having the same pattern corresponding to the lateral and longitudinal partition walls of the partition wall assembly (45).
12. The plasma display panel according to claim 1, wherein protruding portions (11A) of two row electrodes (X, Y) forming one displaying line (L) have mutually facing head portions which are inclined with respect to the row direction of the panel.
13. The plasma display panel according to claim 1, wherein each displaying line (L) includes a plurality of discharge cells repeatedly arranged in the order of R, G, B, each column includes a plurality of same color discharge cells, with every three discharge cells C (R, G, B) arranged in a display line forming one picture element (GA).
14. The plasma display panel according to claim 1, wherein each displaying line (L) includes a plurality of discharge cells C repeatedly arranged in the order of R, G, B, one displaying line being deviated in the row direction from its adjacent displaying line by

one discharge cell, with every three discharge cells C (R, G, B) arranged in a display line forming one picture element (GB).

15. The plasma display panel according to claim 1, wherein each displaying line includes a plurality of discharge cells C repeatedly arranged in the order of R, G, B, one displaying line being deviated in the row direction from its adjacent displaying line by half width of one discharge cell, with every three discharge cells C (R, G, B) arranged in a display line forming one picture element.
16. The plasma display panel according to claim 1, wherein each displaying line includes a plurality of discharge cells C repeatedly arranged in the order of R, G, B, one displaying line being deviated in the row direction from its adjacent displaying line by 1.5 times the width of one discharge cell, in a manner such that each pitch element (GD) may also be formed by three discharge cells C (R, G, B) which together form a triangular configuration bridging over two mutually adjacent displaying lines (L).
17. The plasma display panel according to claim 1, wherein each lateral partition wall (65b) of the partition wall assembly is divided into two portions (65b', 65b'') by an elongated slot (SL) extending in the row direction of the panel.
18. The plasma display panel according to claim 17, wherein each divided portion of each lateral partition wall (65b) has substantially the same width as that of each longitudinal partition wall (65a) of the partition wall assembly (65).
19. The plasma display panel according to claim 17, wherein a plurality of light absorbing straps (70) are formed on the inner surface of the front substrate (10), in positions corresponding to the elongated slots (SL).
20. The plasma display panel according to claim 17, wherein a plurality of light absorbing straps (70) are formed on the inner surface of the front substrate (10), in positions corresponding to the longitudinal partition walls (65a) of the partition wall assembly (65).
21. The plasma display panel according to claim 17, wherein at least the longitudinal partition walls (65a) of the partition wall assembly (65) have a two-layer structure, one of which is a light absorbing layer facing toward the front substrate (10), and the other of which is a light reflecting layer facing toward the rear substrate (13).
22. The plasma display panel according to claim 1,

wherein each of two row electrodes (X, Y) of a row electrode pair includes an elongated main body portion extending in the row direction of the panel and a plurality of protruding portions (11A) extending in the column direction of the panel, so that a plurality of discharge gaps (g) are formed between mutually facing protruding portions of two elongated main body portions,

wherein each elongated main body portion is made by a metal film;

wherein each protruding portion (11A) is formed by a transparent electrically conductive film, with its base end connected to an elongated main body portion.

23. The plasma display panel according to claim 22, wherein a light absorbing layer is formed on each elongated main body portion so that said light absorbing layer is interposed between the inner surface of the front substrate (10) and the elongated main body portion.
24. The plasma display panel according to claim 22, wherein one elongated main body portion is shared by two mutually adjacent row electrodes (Xi, Xi+1, Yi'+ Yi+1') of two mutually adjacent displaying lines (Li-1', Li').
25. The plasma display panel according to claim 17, wherein the outermost corner portions of each lateral partition wall are removed so as to form inclined surfaces thereon.
26. The plasma display panel according to claim 1 or 17, wherein outer end portions of partition wall assembly (105) are formed in positions not facing the projection portions (11A) of the dielectric layer (11).
27. The plasma display panel according to claim 26, wherein outer end portions of each pair of lateral partition walls (105b) are combined with each other in positions not facing the projection portions of the dielectric layer (11).
28. The plasma display panel according to claim 1, wherein the partition wall assembly is made of a light transmissible material.
29. A plasma display panel comprising:
 - a front substrate (10);
 - a plurality of row electrode pairs (X, Y) provided on the inner surface of the front substrate (10), said row electrode pairs (X, Y) being arranged in parallel with one another and extending in the

row direction of the panel with each row electrode pair (X, Y) forming a displaying line (L);

a dielectric layer (11) provided on the inner surface of the front substrate (10) for covering the row electrode pairs (X, Y);

a rear substrate (13) arranged in parallel with and space-apart from the front substrate (10), forming a discharge space (S) therebetween;

a plurality of column electrodes (D) provided on the inner surface of the rear substrate (13), said column electrodes (D) being arranged in parallel with one another and extending in the column direction of the panel in a manner such that at each intersection of a row electrode pair (X, Y) with a column electrode (D) there is formed a light emission unit

wherein each of two row electrodes of one row electrode pair (X, Y) has a plurality of protruding portions (11A), thereby forming a plurality of discharge gaps (g) between mutually facing protruding portions of the two row electrodes (X, Y);

wherein a mutual positional relationship between two row electrodes (X, Y) of one row electrode pair is alternatively changed from one displaying line (L) to another;

one common electrode main body portion is shared by two mutually adjacent row electrodes (Xi, Xi+1, Yi, Yi+1) of two mutually adjacent displaying lines (Li-1, Li).

30. A method of making a plasma display panel comprising:

arranging a plurality of row electrode pairs (X, Y), provided on the inner surface of a front substrate (10), in parallel with one another and extending in the row direction of the panel, with each row electrode pair (X, Y) forming a displaying line (L);

providing a dielectric layer (11) on the inner surface of the front substrate (10) for covering the row electrode pairs (X, Y);

arranging a rear substrate (13) in parallel with and space-apart from the front substrate (10), forming a discharge space (S) therebetween;

arranging a plurality of column electrodes (D), provided on the inner surface of the rear substrate (13), in parallel with one another and ex-

tending in the column direction of the panel, in a manner such that at each intersection of a row electrode pair (X, Y) with a column electrode (D) there is formed a light emission unit;

providing a partition wall assembly (15) between the front substrate (10) and the rear substrate (13), said partition wall assembly (15) including a plurality of longitudinal partition walls (15a) and a plurality of lateral partition walls (15b), thereby dividing the discharge space (S) into a plurality of discharge cells (C);

wherein the dielectric layer (11) has a plurality of projection portions (11A) located corresponding to and protruding toward the lateral partition walls (15b) of the partition wall assembly (15), in a manner such that there would be no slots formed between the dielectric layer (11) and the lateral partition walls (15b).

31. A method of making a plasma display panel comprising:

arranging a plurality of row electrode pairs (X, Y), provided on the inner surface of a front substrate (10), in parallel with one another and extending in the row direction of the panel, with each row electrode pair (X, Y) forming a displaying line (L);

providing a dielectric layer (11) on the inner surface of the front substrate (10) for covering the row electrode pairs (X, Y);

arranging a rear substrate (13) in parallel with and space-apart from the front substrate (10), forming a discharge space (S) therebetween;

arranging a plurality of column electrodes (D), provided on the inner surface of the rear substrate (13), in parallel with one another and extending in the column direction of the panel, in a manner such that at each intersection of a row electrode pair (X, Y) with a column electrode (D) there is formed a light emission unit;

wherein each of two row electrodes of one row electrode pair (X, Y) has a plurality of protruding portions (11A), thereby forming a plurality of discharge gaps (g) between mutually facing protruding portions of the two row electrodes (X, Y);

wherein a mutual positional relationship between two row electrodes (X, Y) of one row electrode pair is alternatively changed from one displaying line (L) to another;

one common electrode main body portion is shared by two mutually adjacent row electrodes (X_i , X_{i+1} , Y_i' , Y_{i+1}') of two mutually adjacent displaying lines (L_{i-1}' , L_i').

5

10

15

20

25

30

35

40

45

50

55

Fig.2

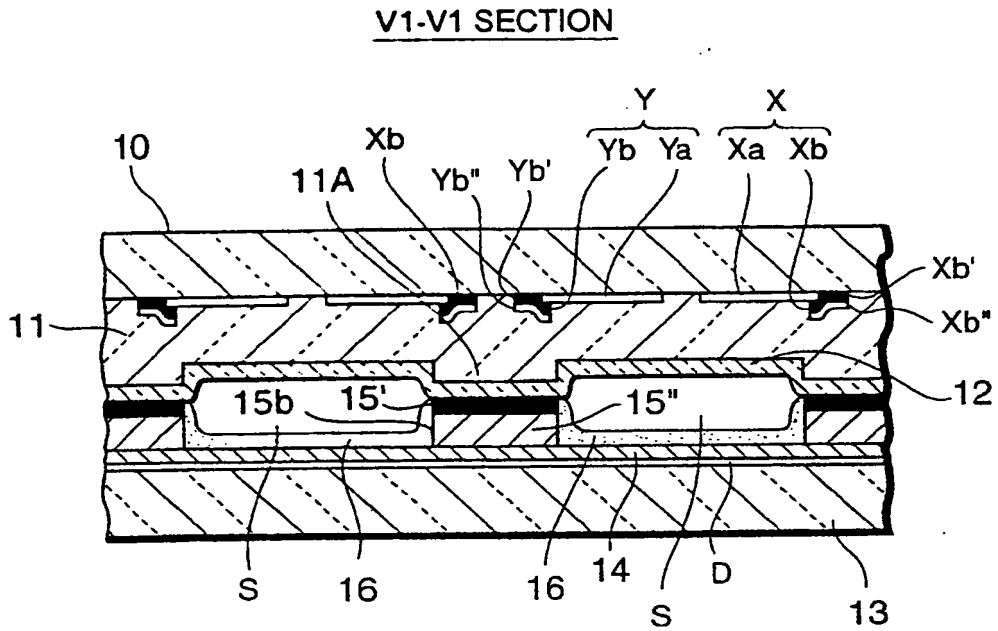


Fig.3

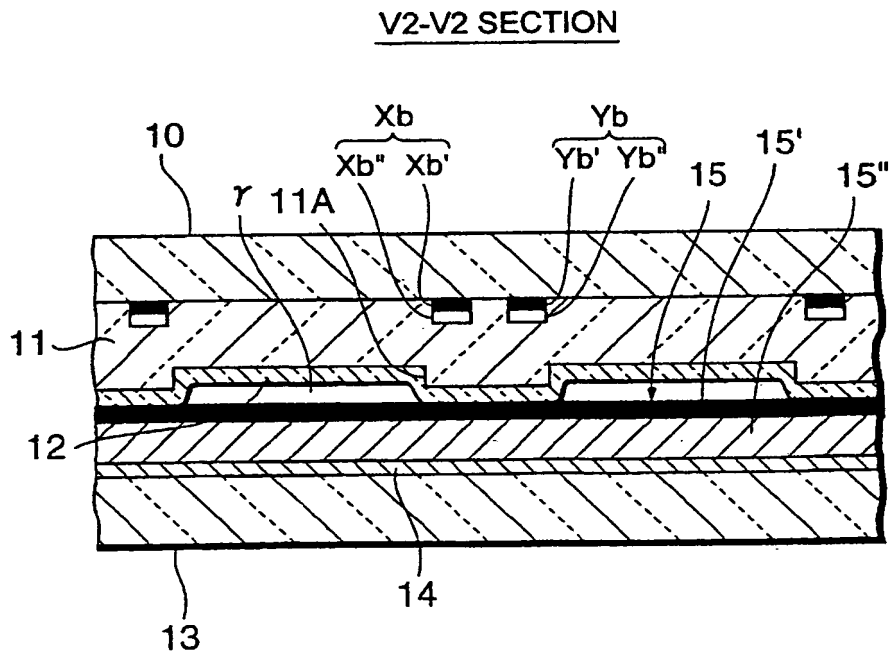


Fig.4

W1-W1 SECTION

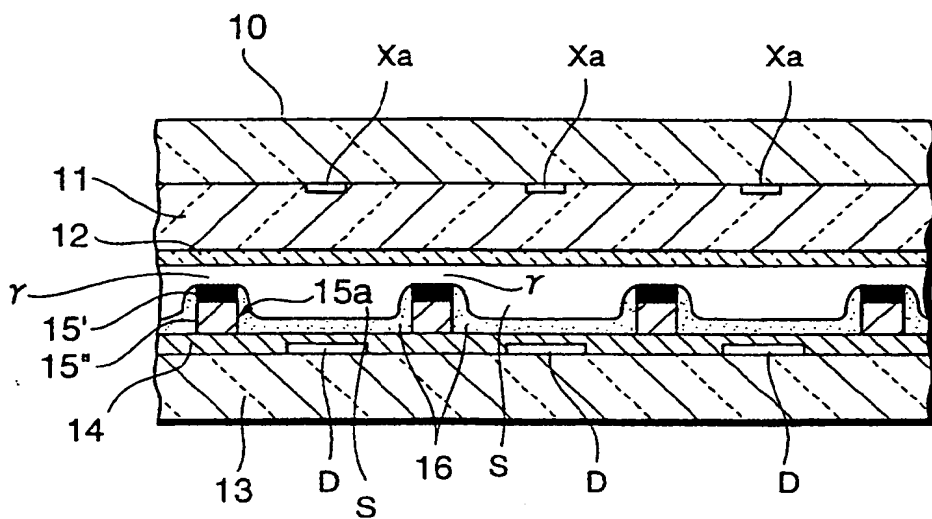


Fig.5

W2-W2 SECTION

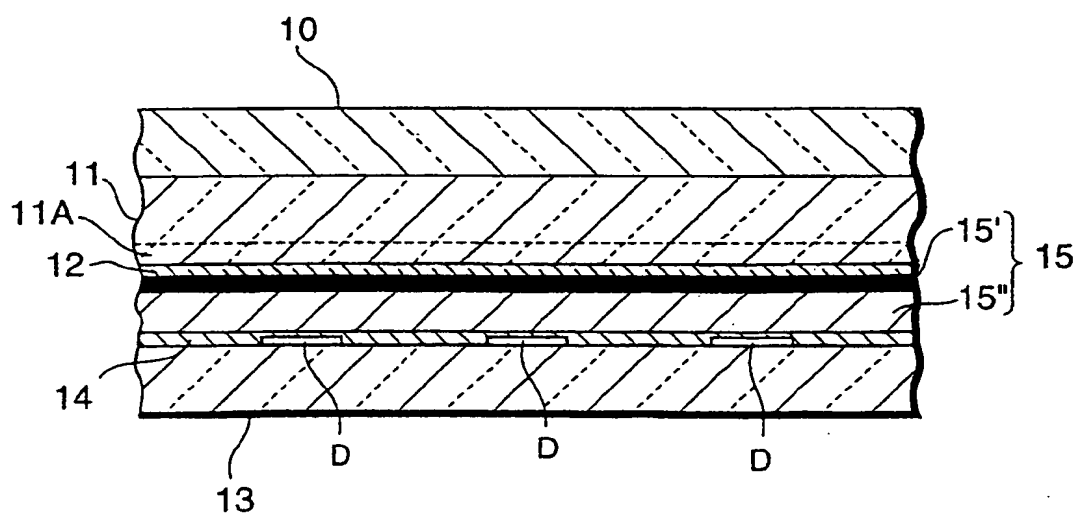


Fig.6

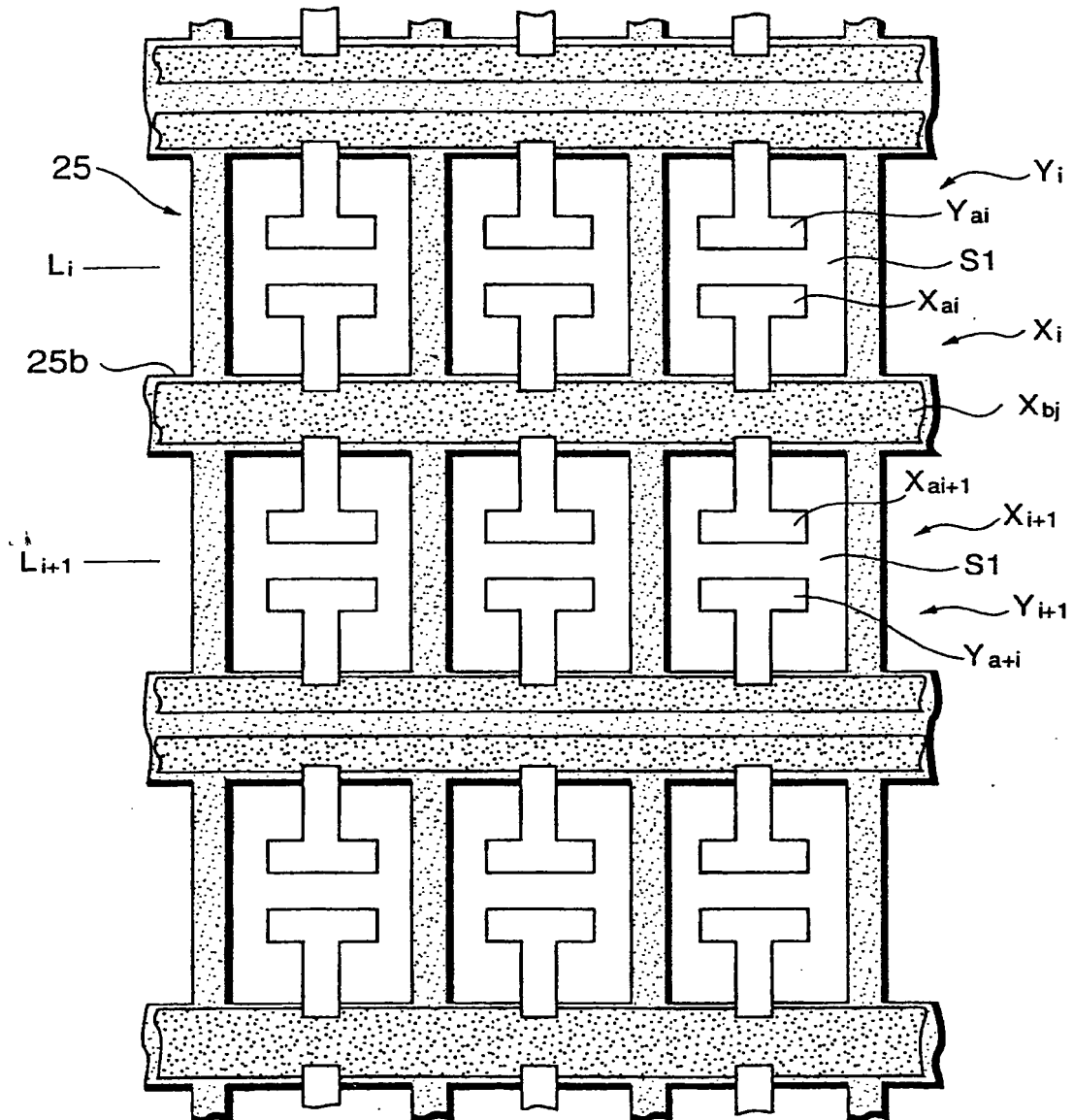


Fig.7

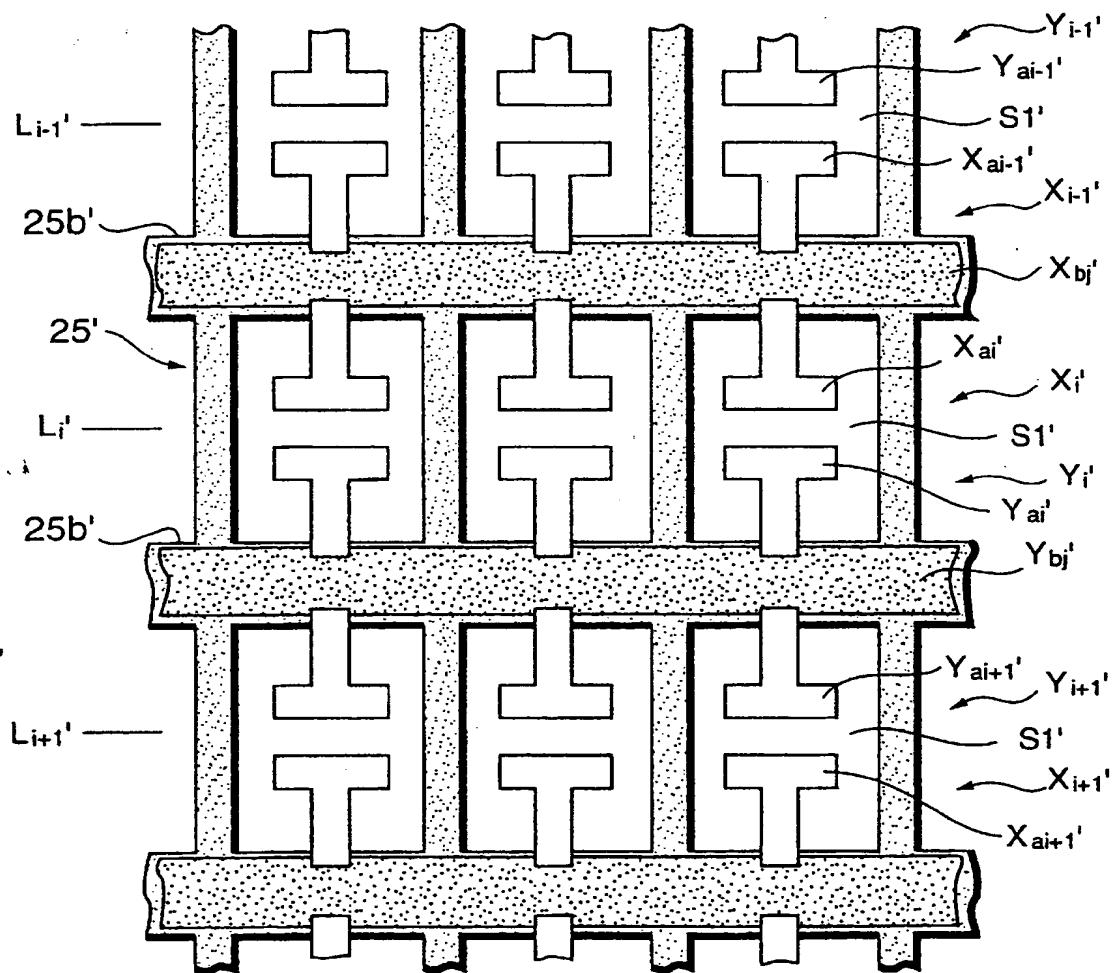
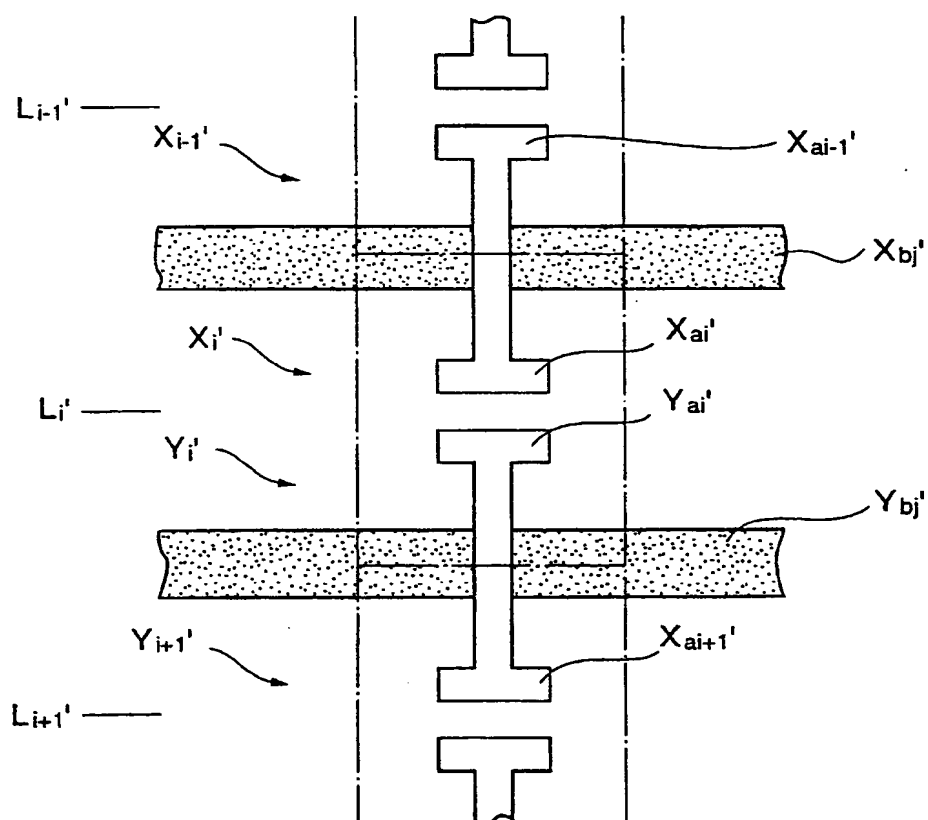


Fig.8



MEMPHIS, TENN 4017001A9 I L

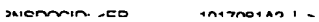


Fig.10

V3-V3 SECTION

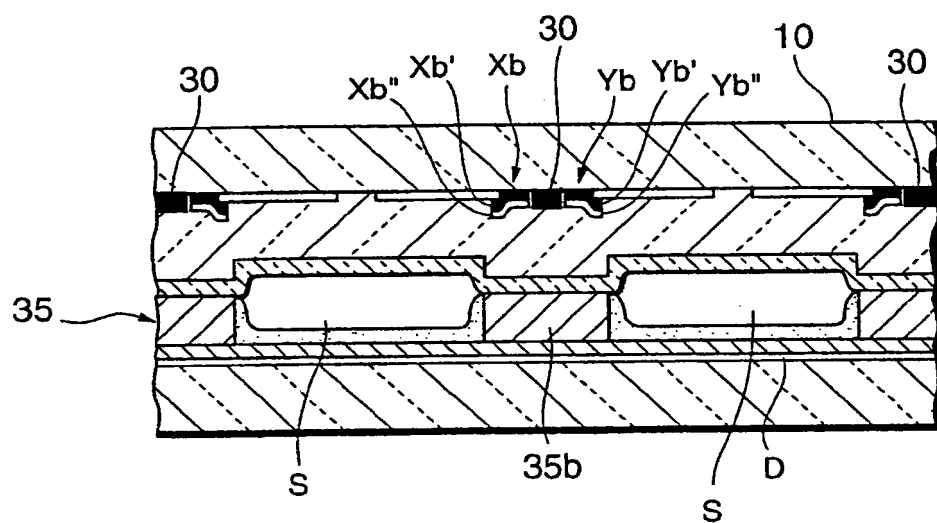


Fig.11

V4-V4 SECTION

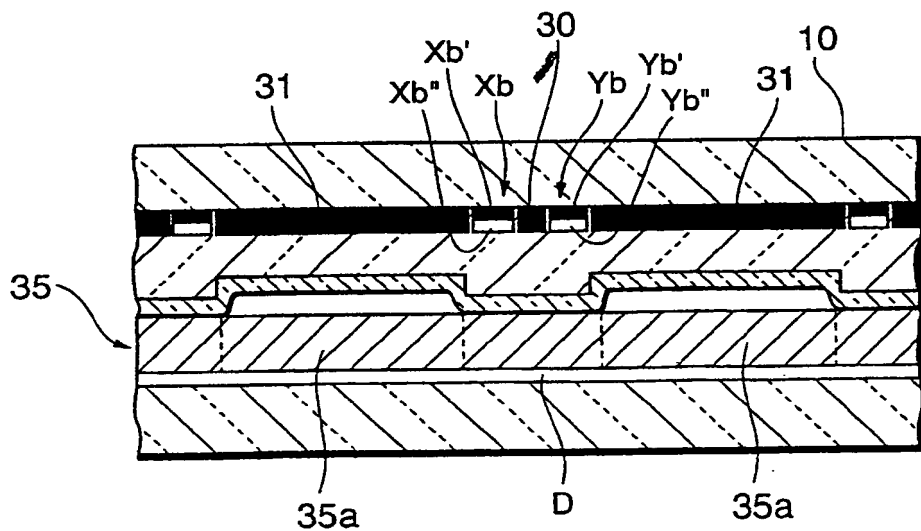


Fig. 12

W3-W3 SECTION

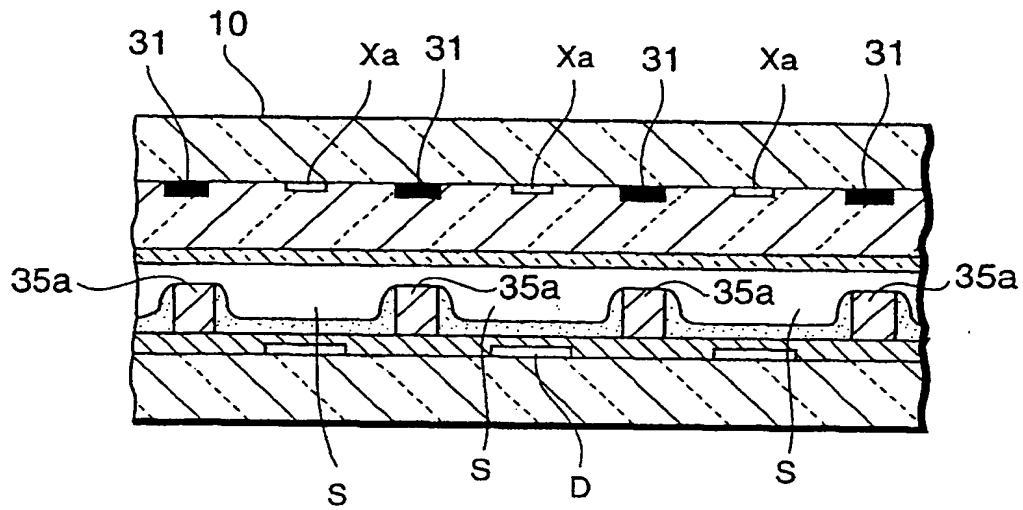


Fig. 13

W4-W4 SECTION

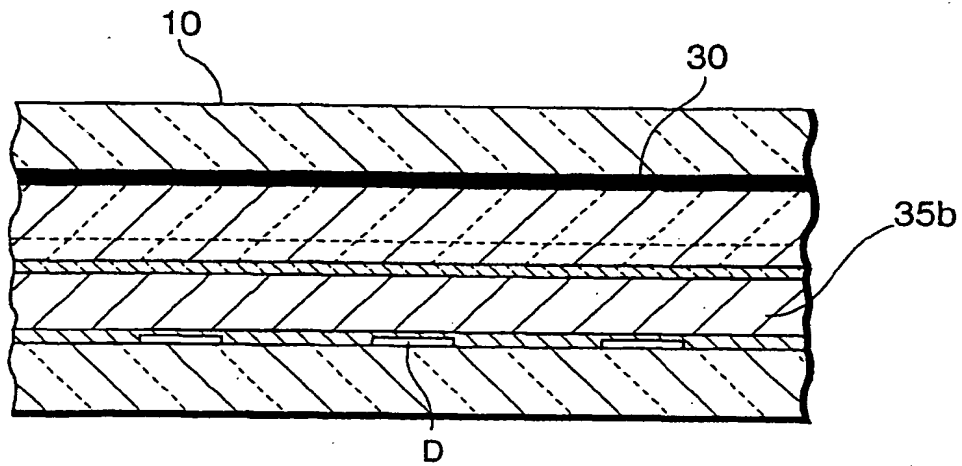


Fig. 14

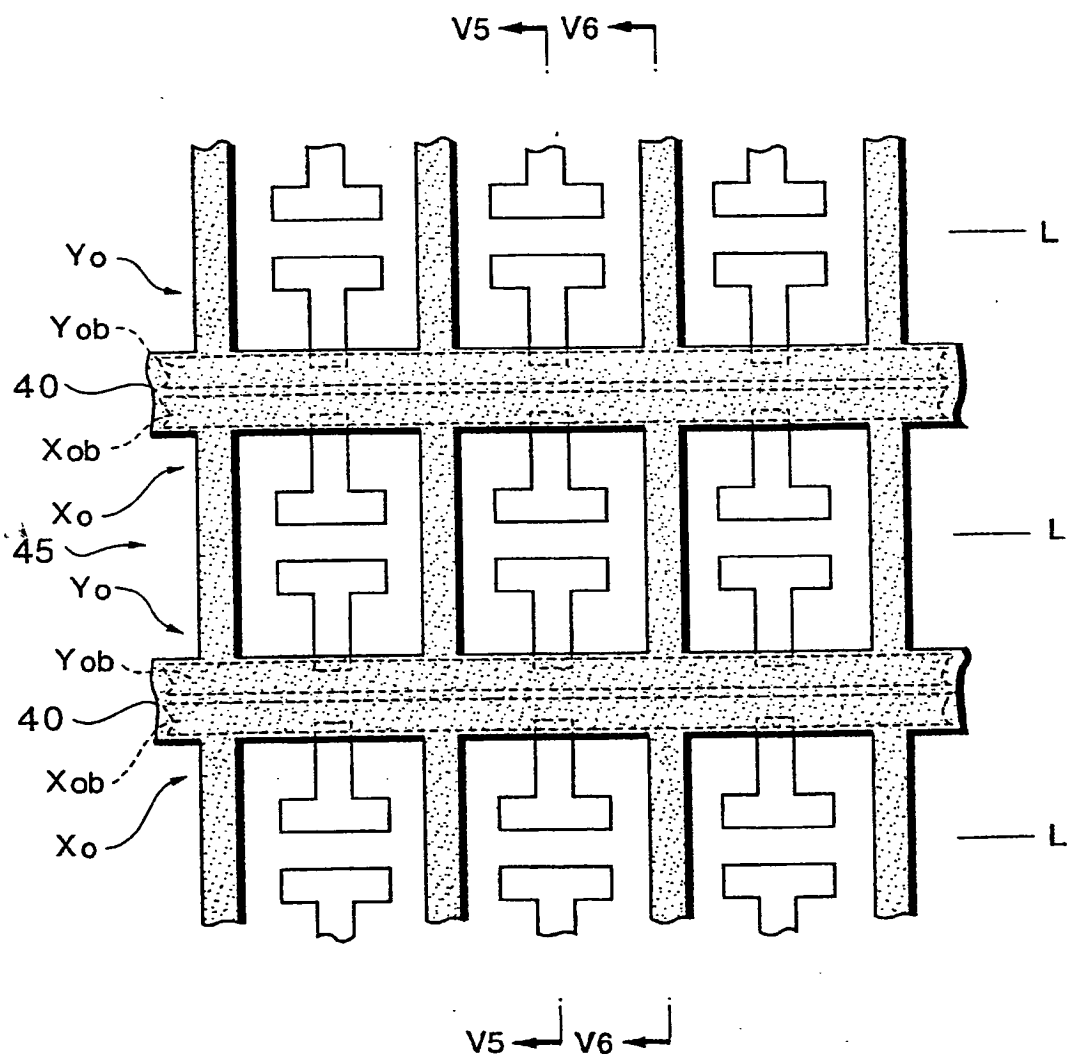


Fig.15

V5-V5 SECTION

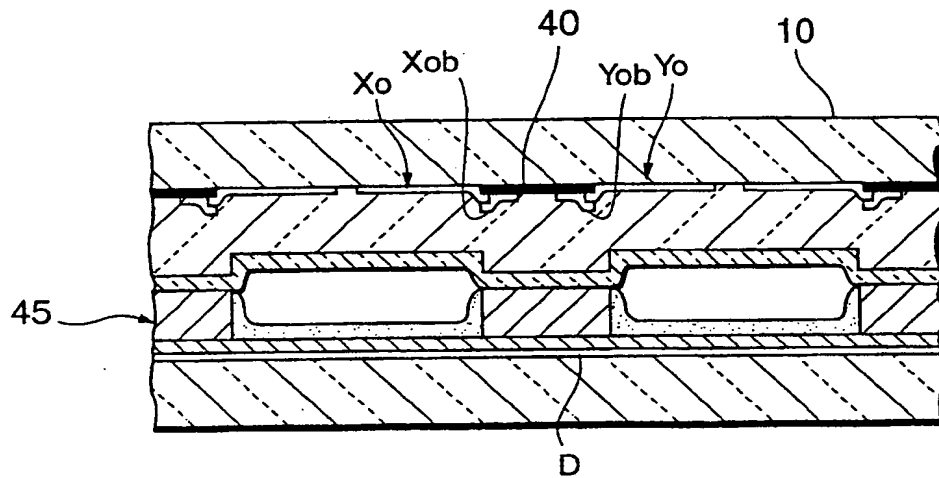


Fig.16

V6-V6 SECTION

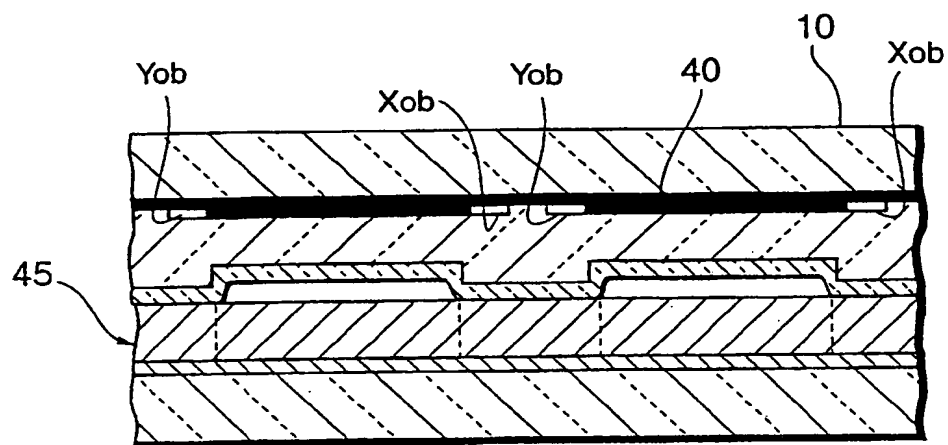


Fig.18

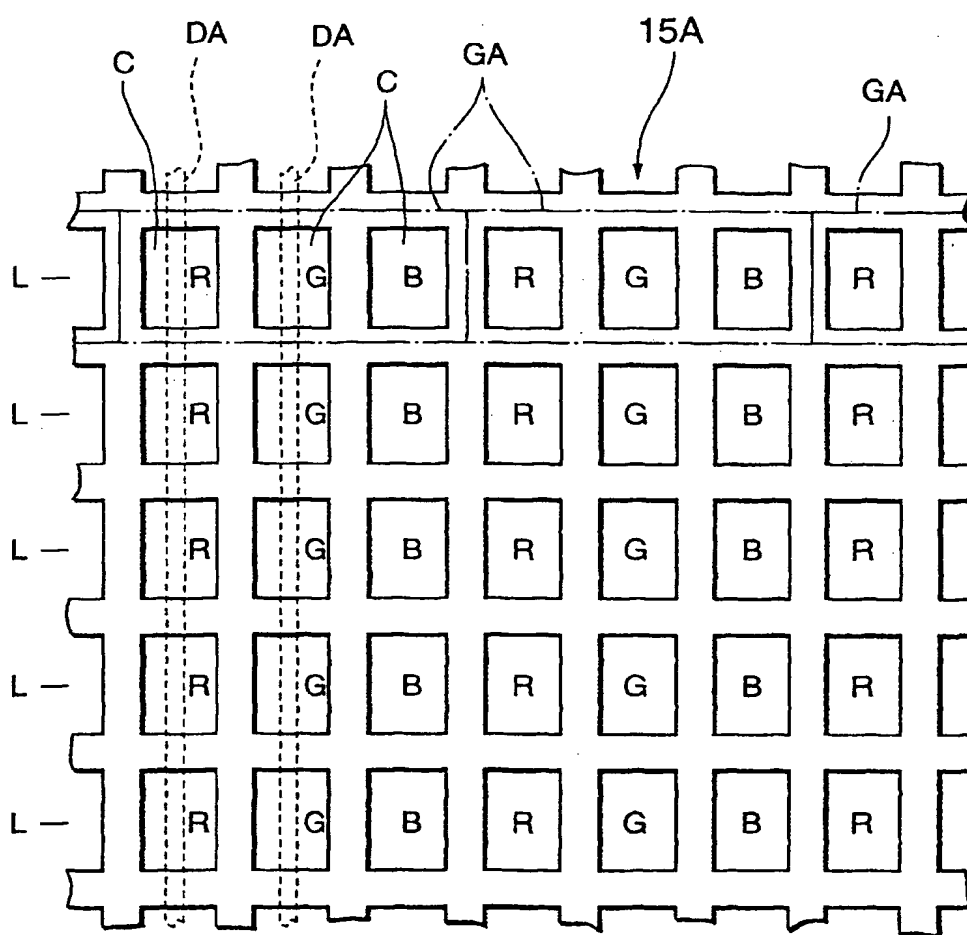


Fig. 19

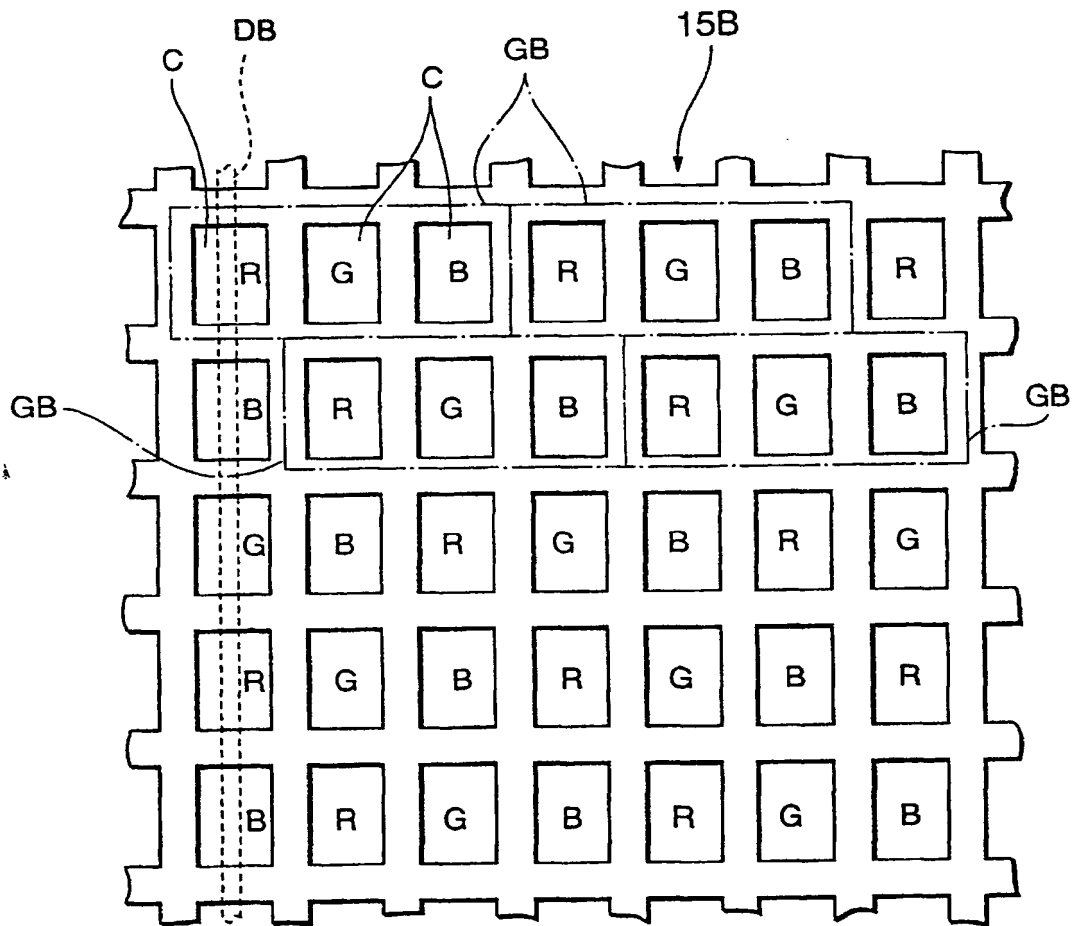


Fig.20

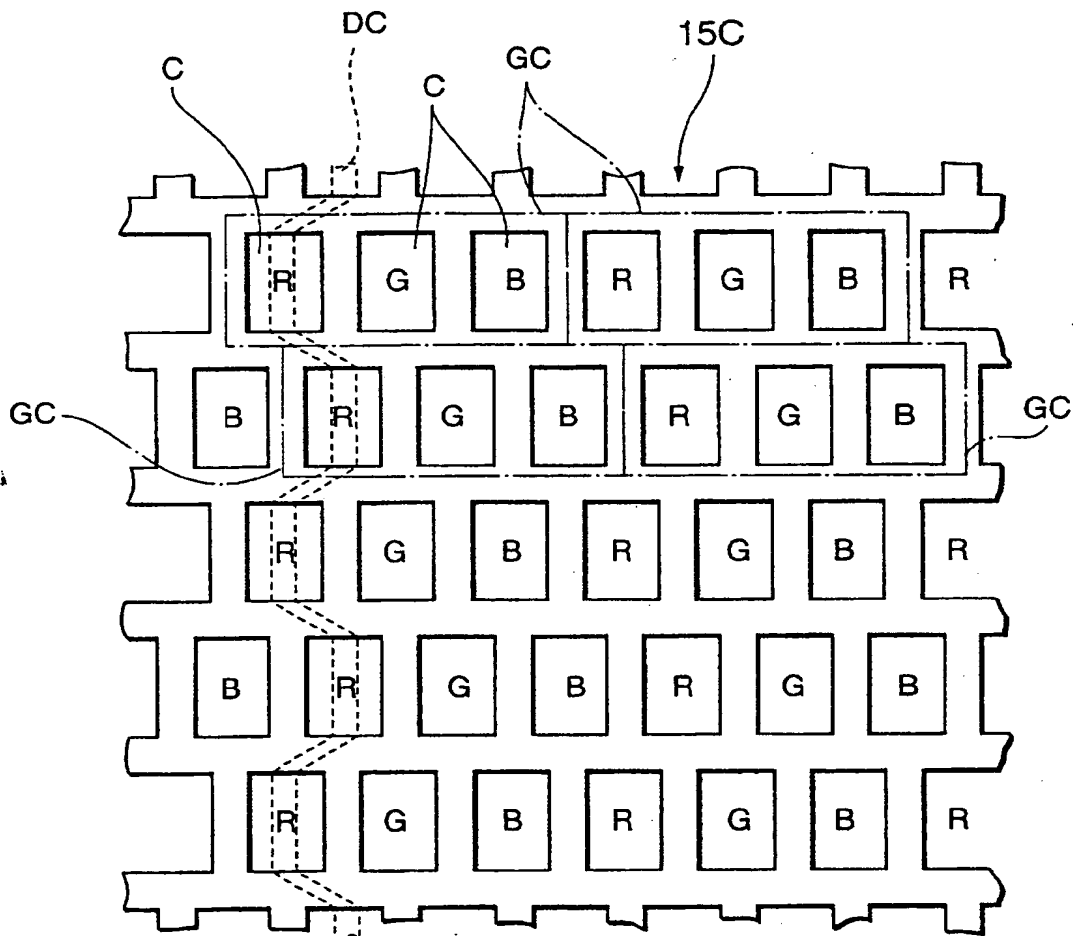


Fig.21

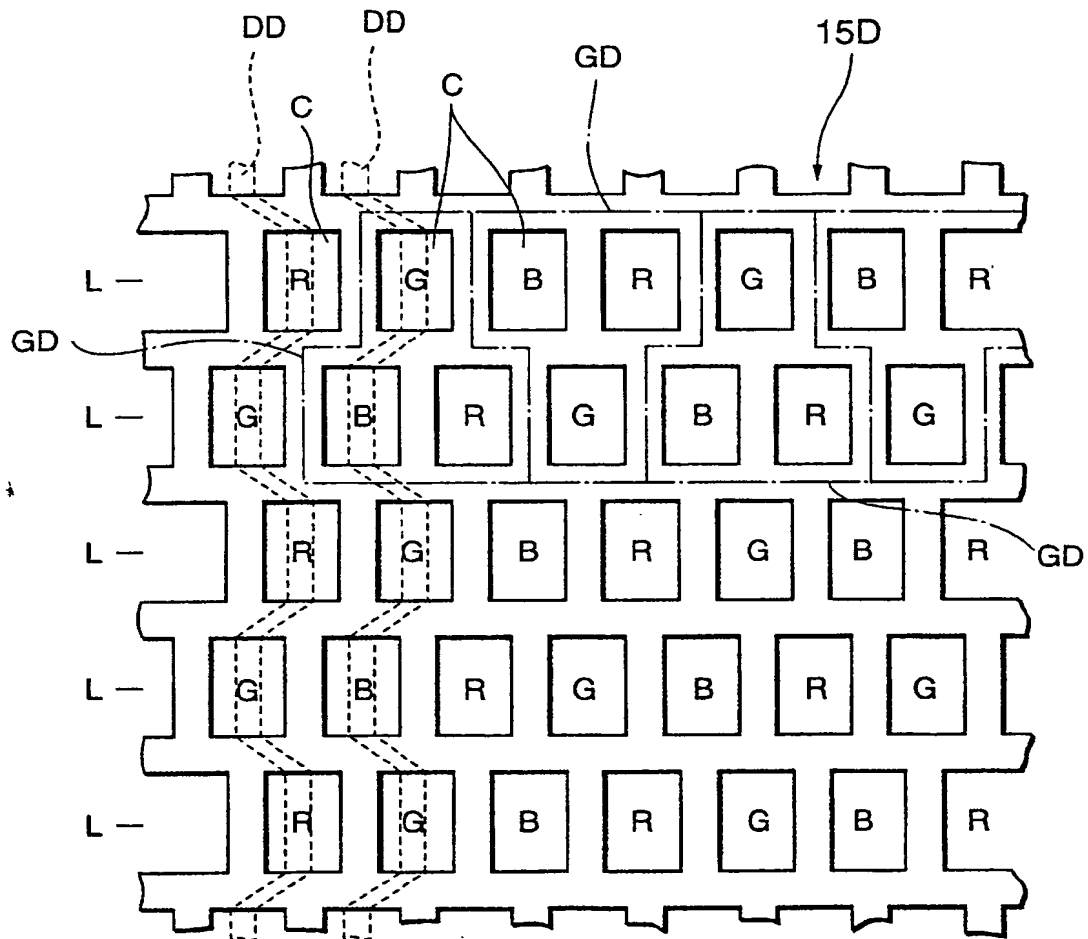


Fig.22

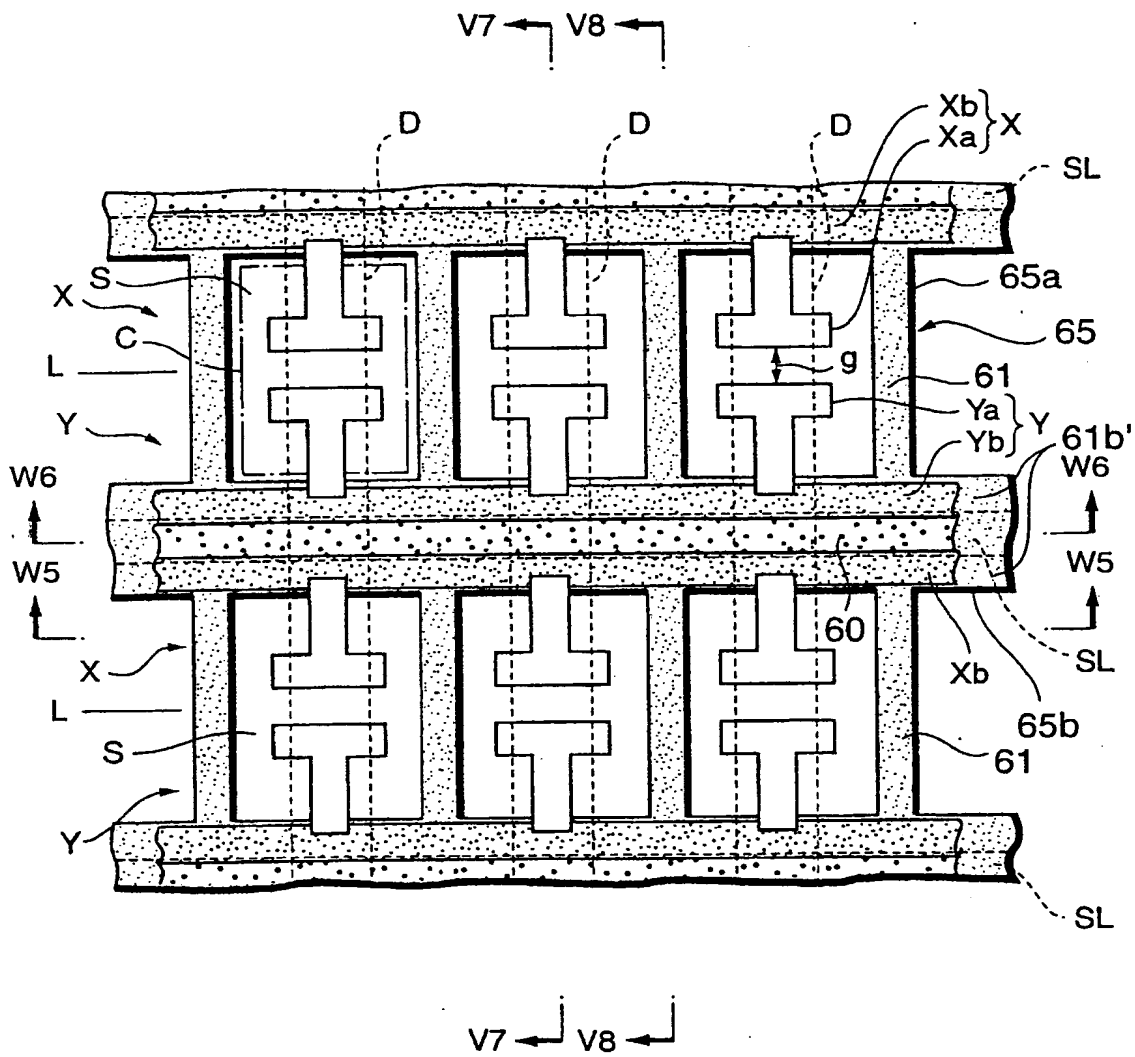


Fig.23

V7-V7 SECTION

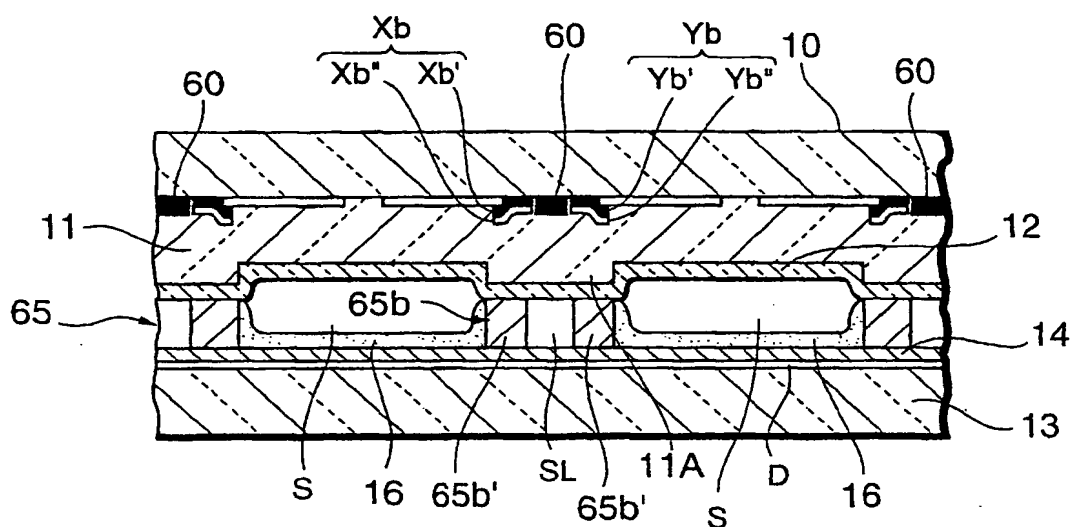


Fig.24

V8-V8 SECTION

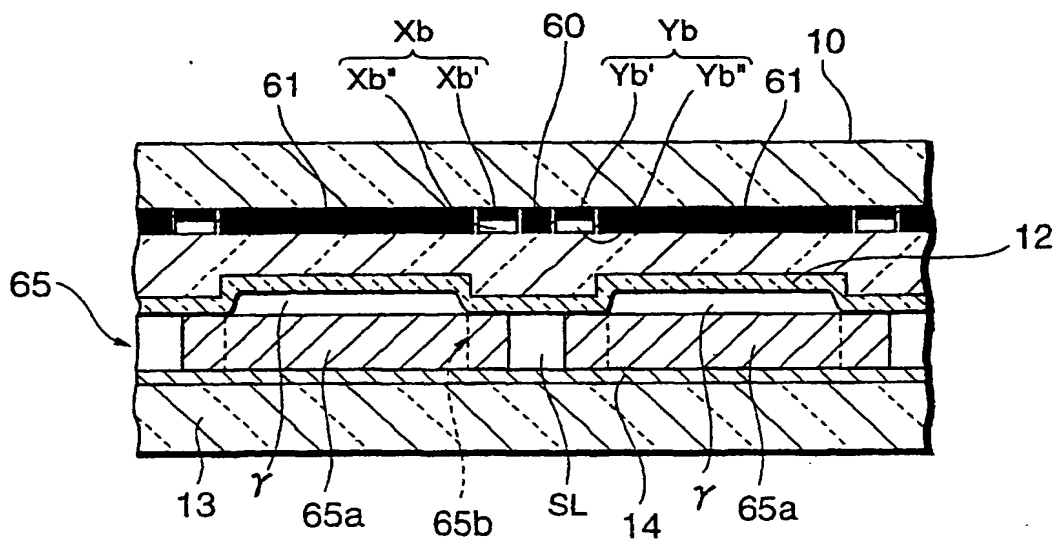


Fig.25

W5-W5 SECTION

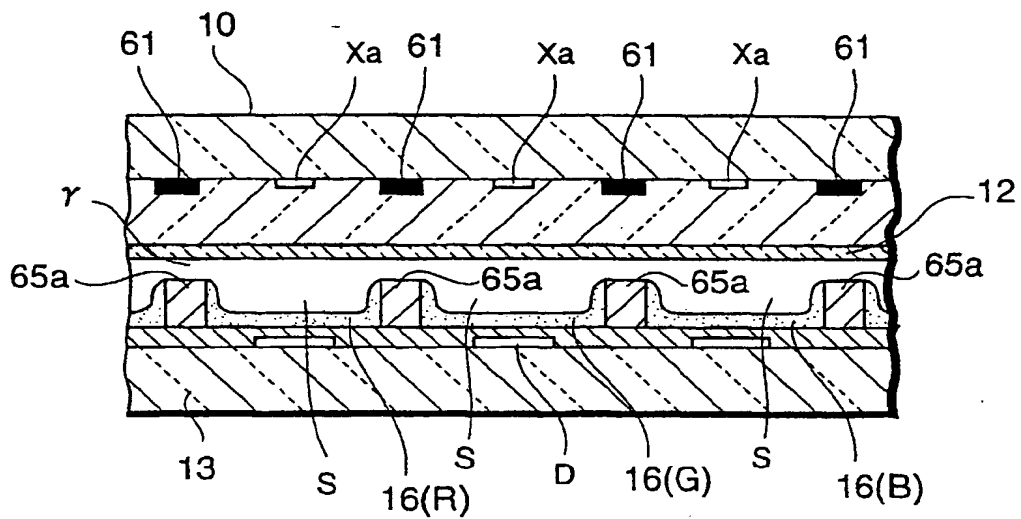


Fig.26

W6-W6 SECTION

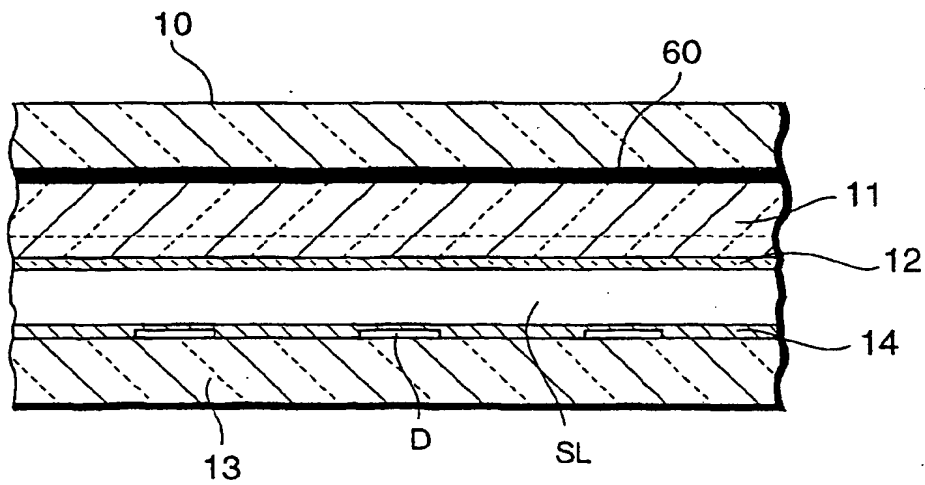


Fig.27

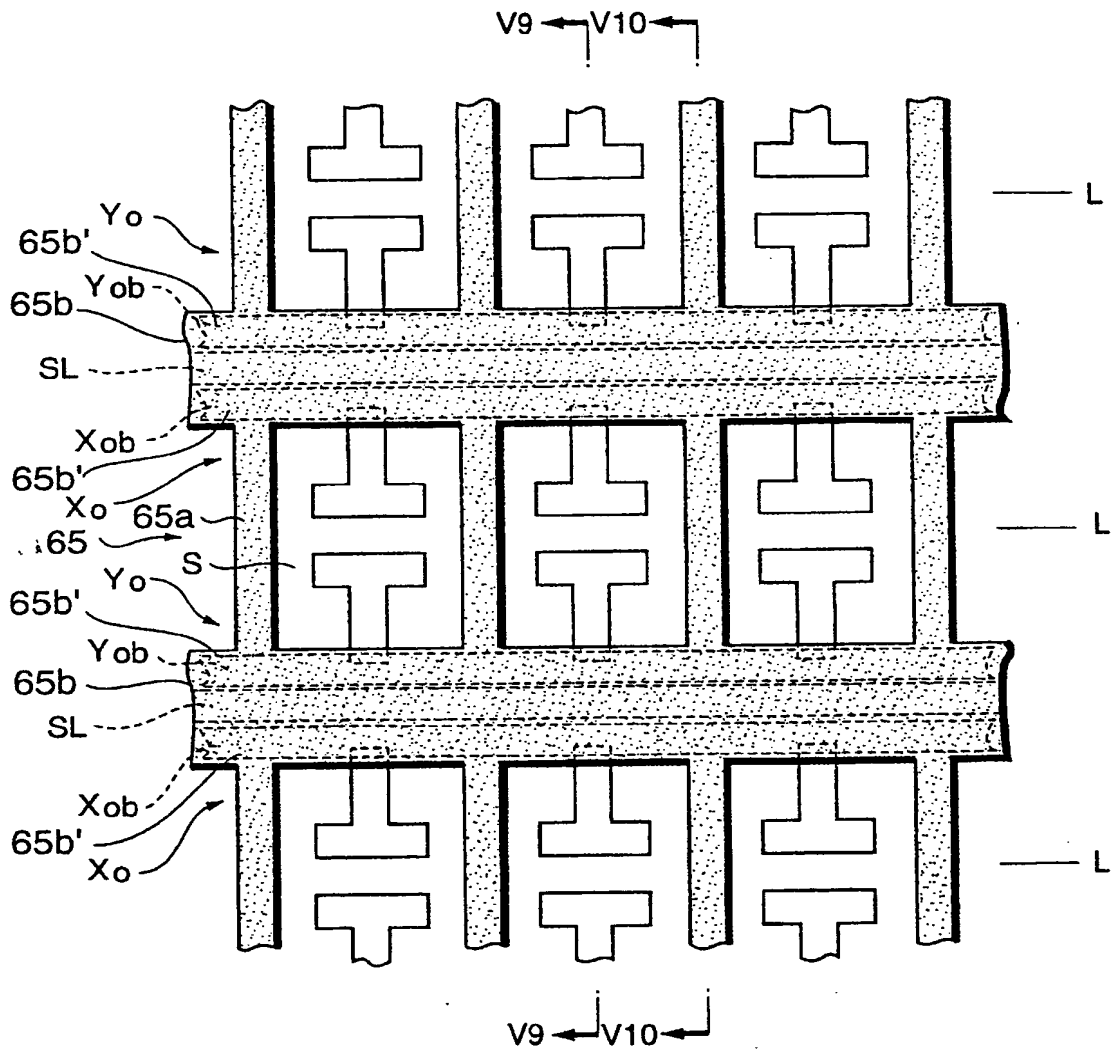


Fig.28

V9-V9 SECTION

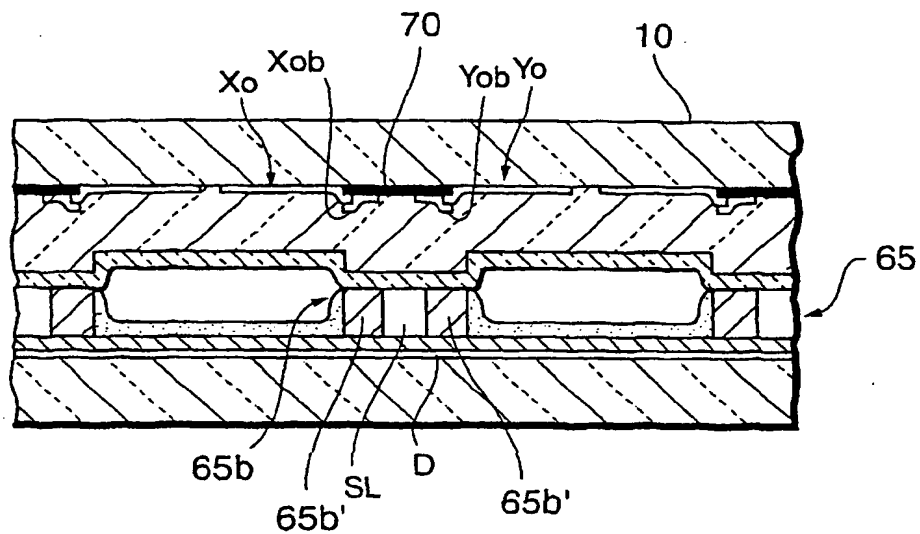
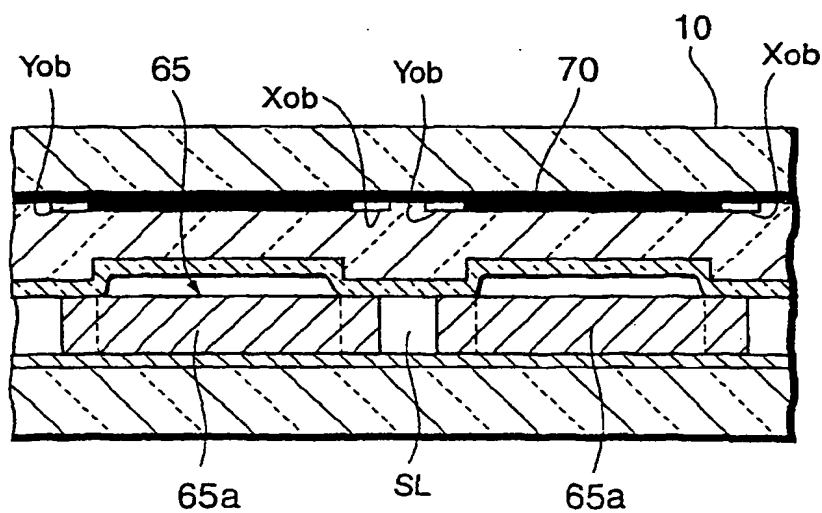


Fig.29

V10-V10 SECTION



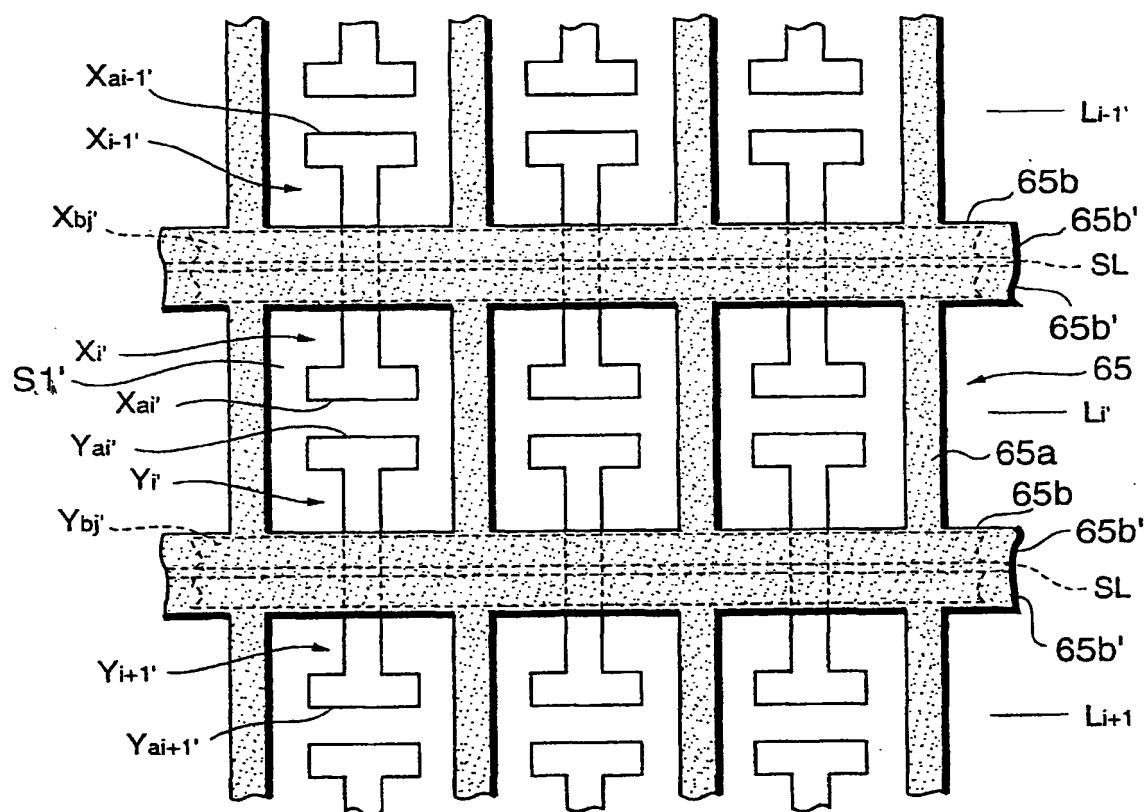


Fig.31

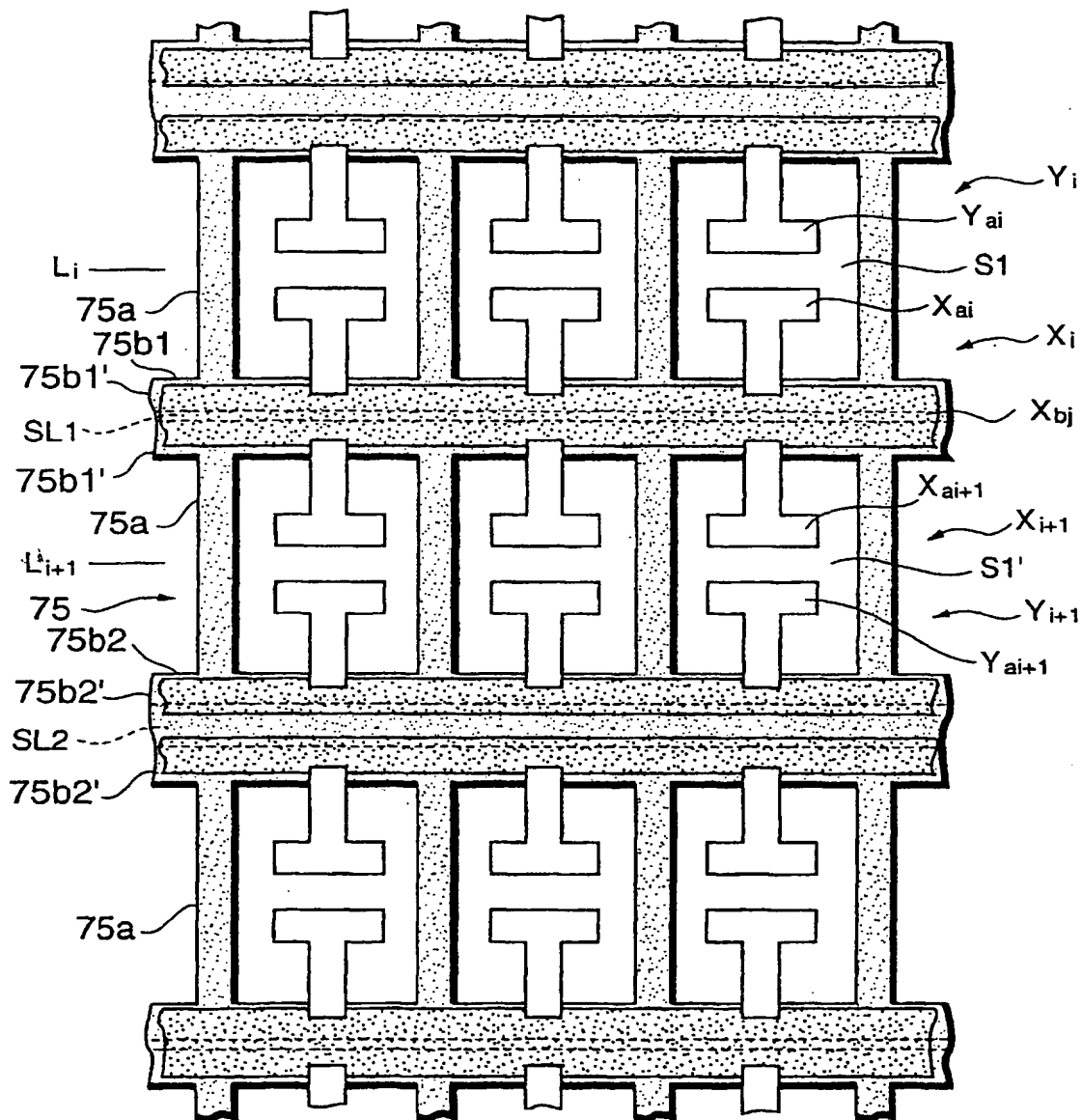


Fig.32

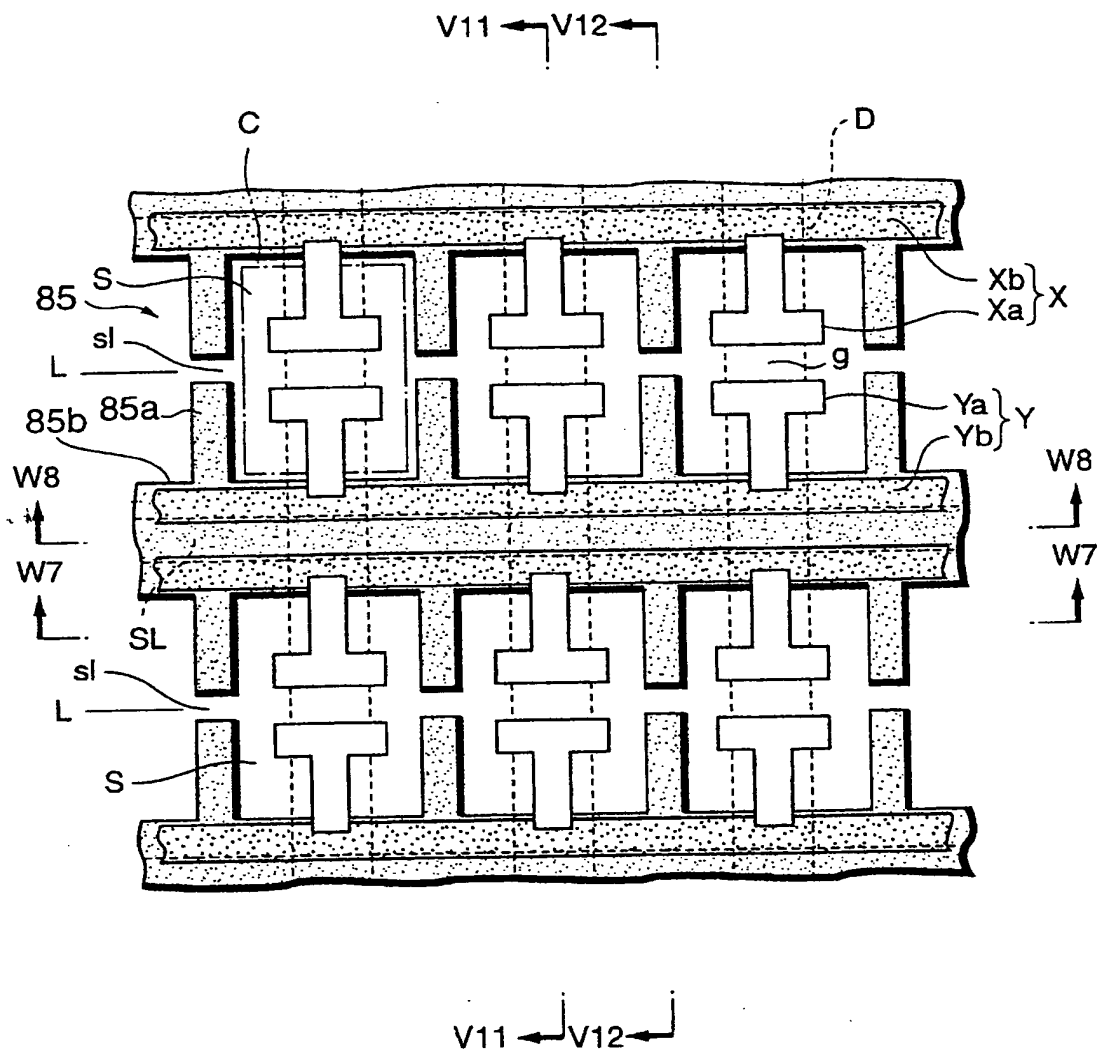


Fig.33

V11-V11 SECTION

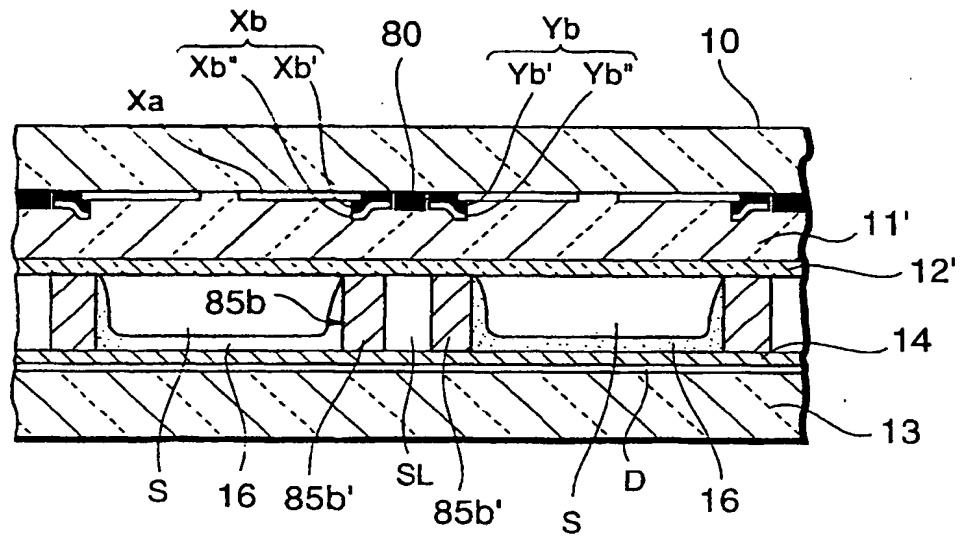


Fig.34

V12-V12 SECTION

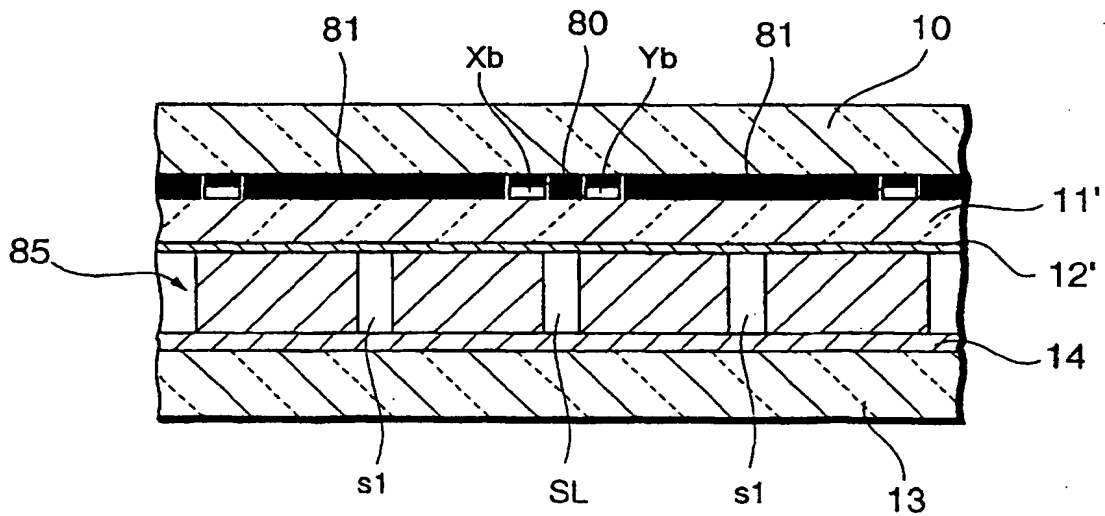


Fig.35

W7-W7 SECTION

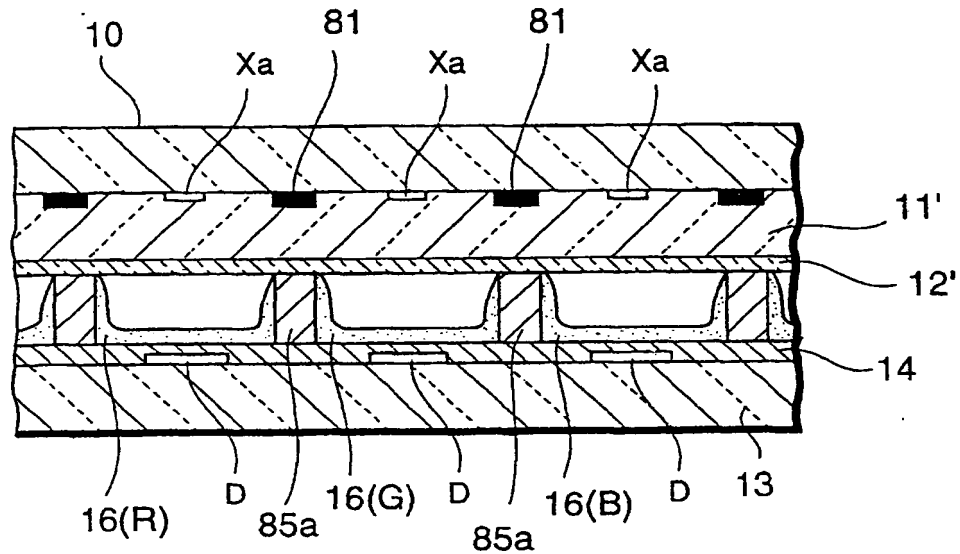


Fig.36

W8-W8 SECTION

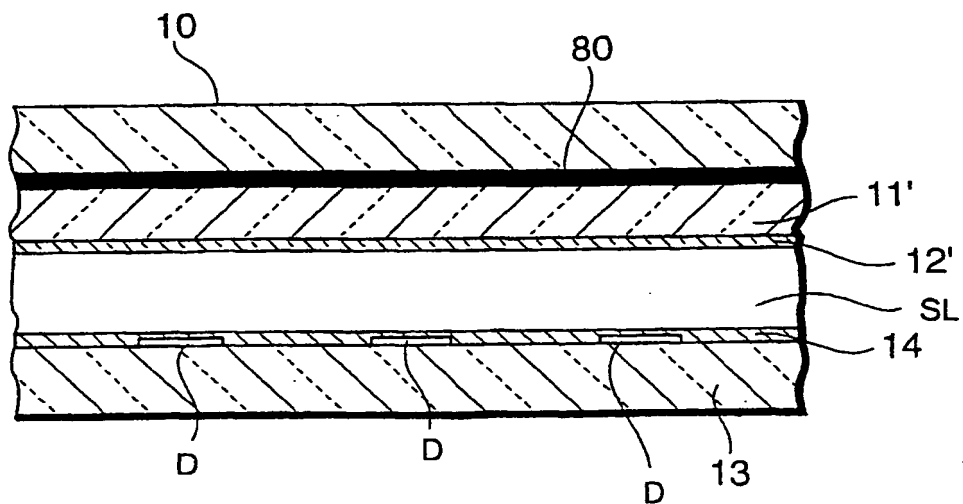


Fig.37

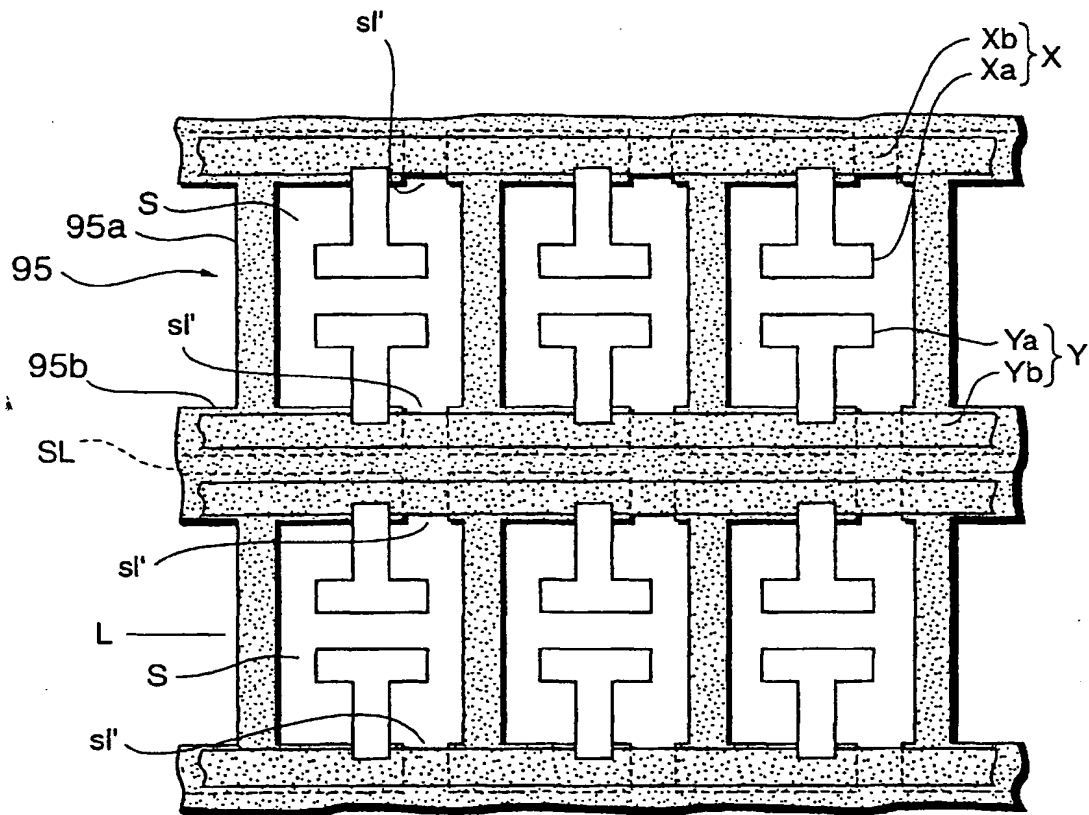


Fig.38

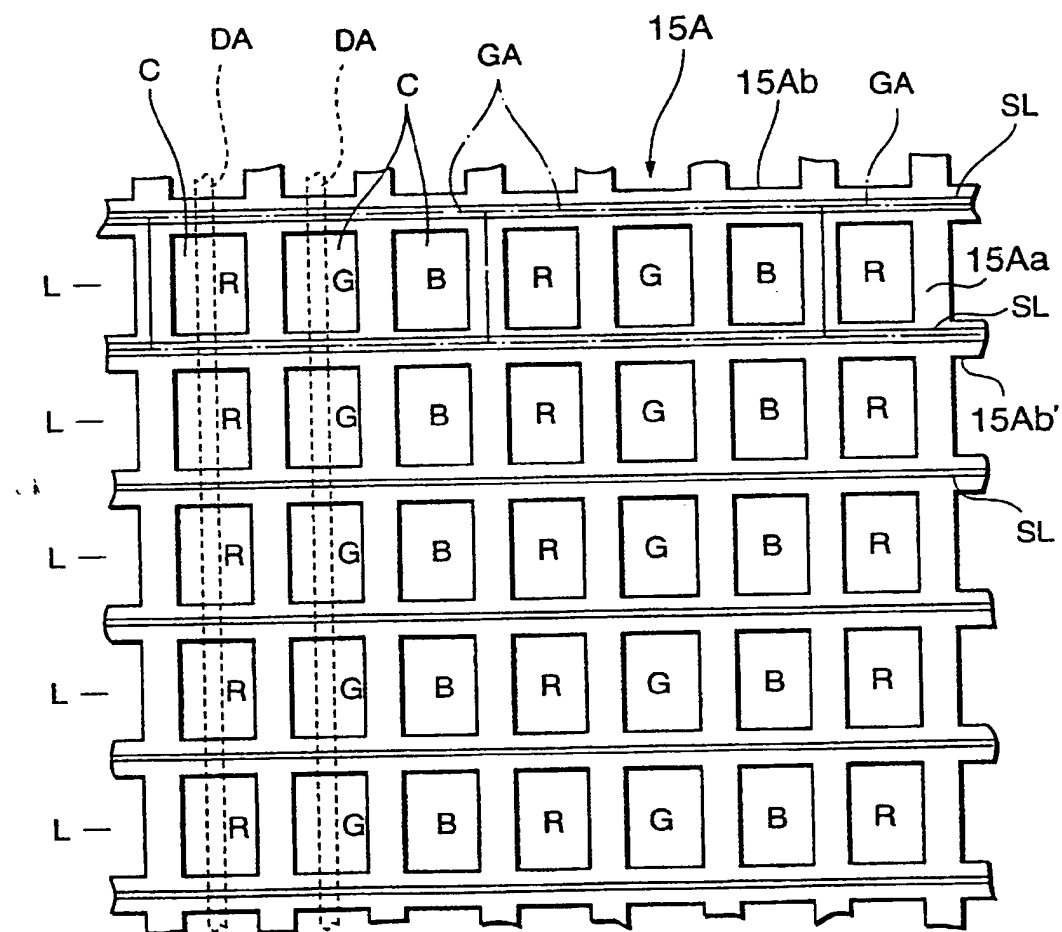


Fig.39

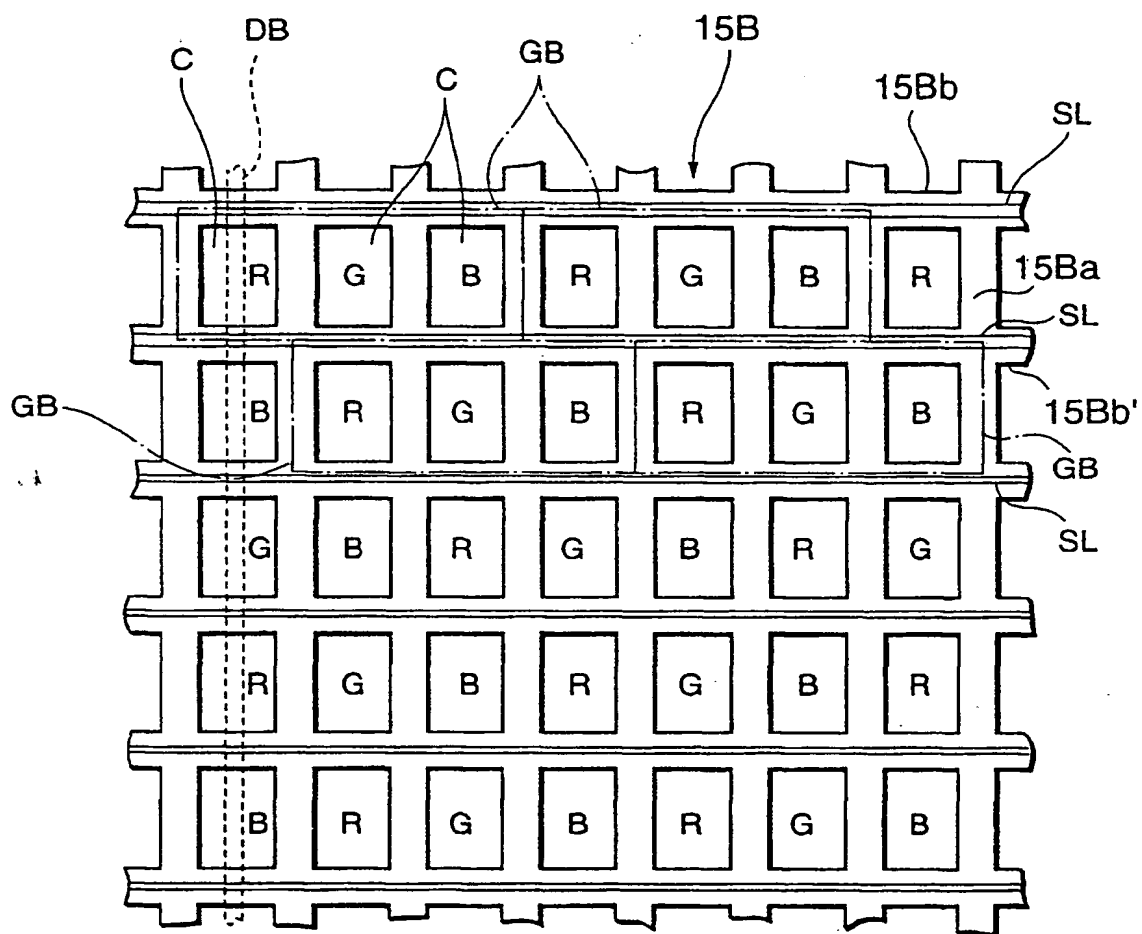


Fig.40

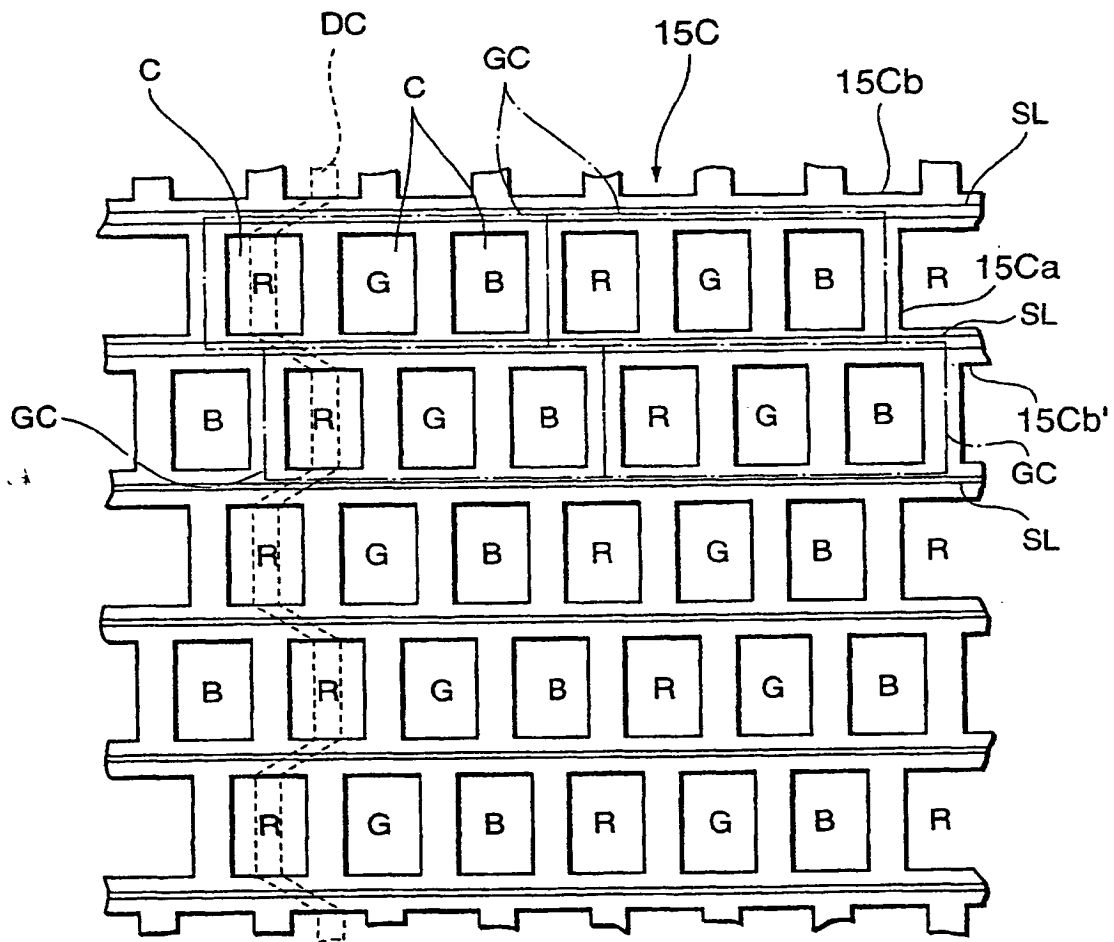


Fig.41

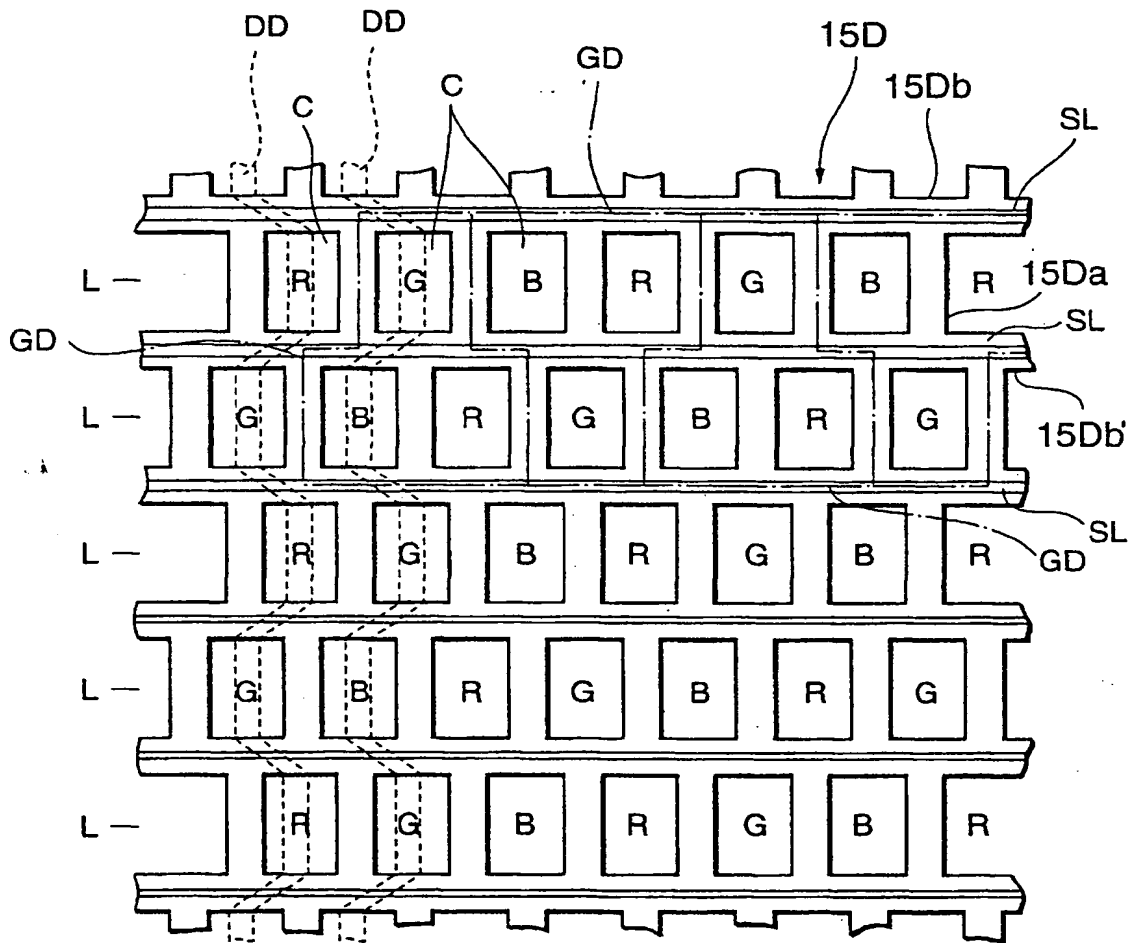


Fig. 42

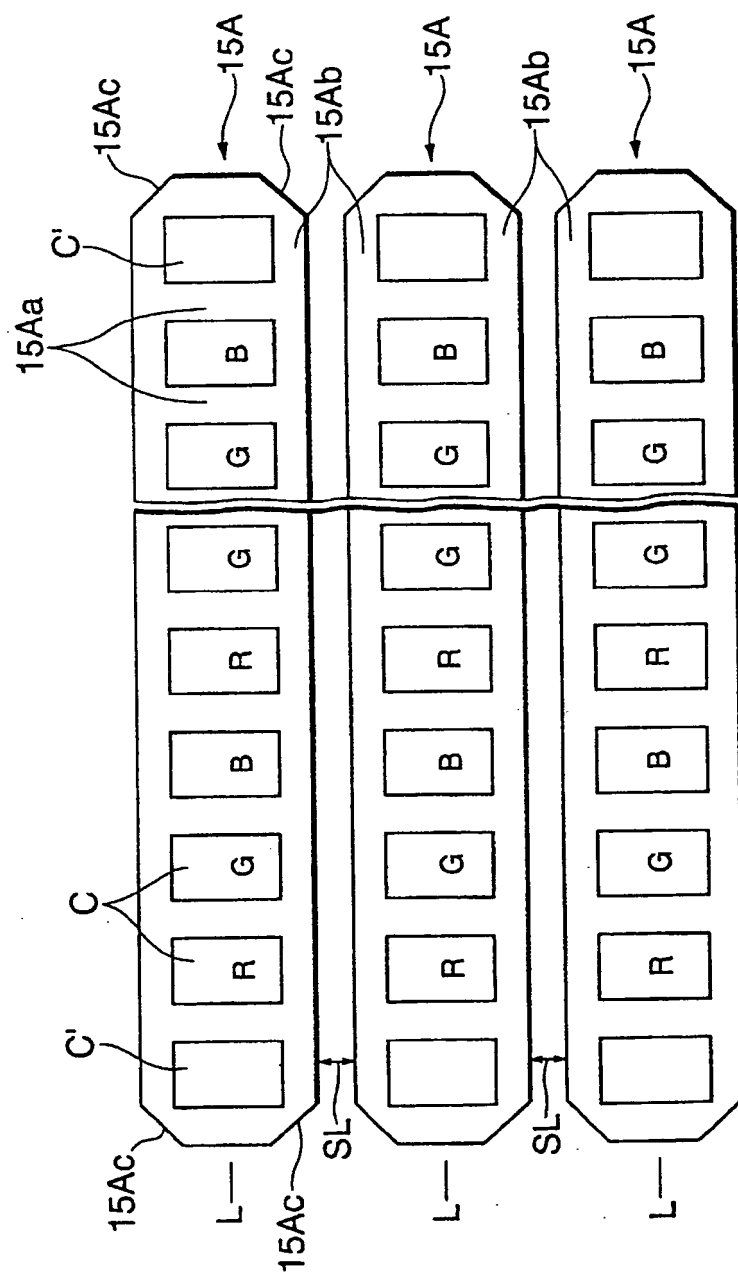


Fig. 43

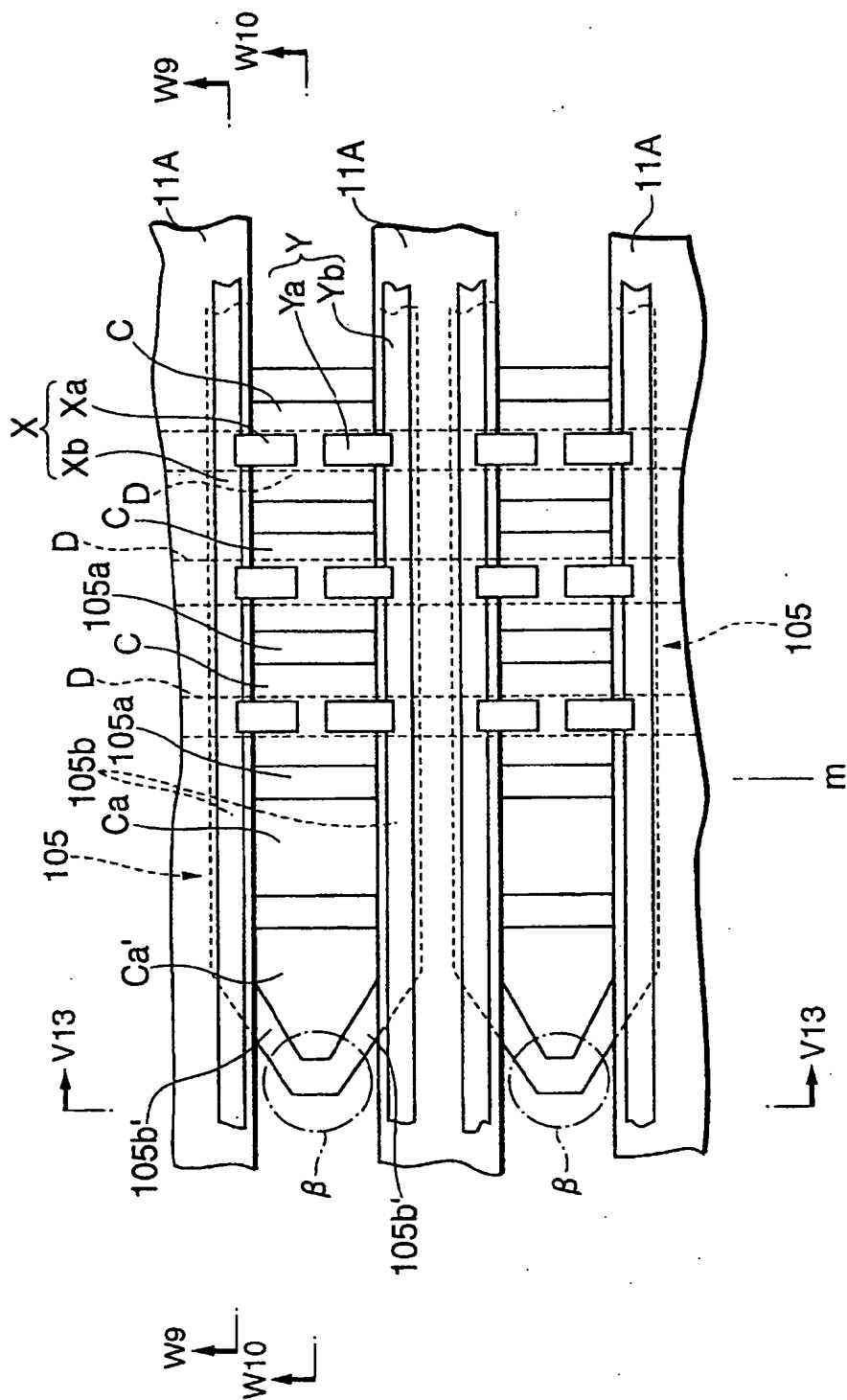


Fig.44

W9-W9 SECTION

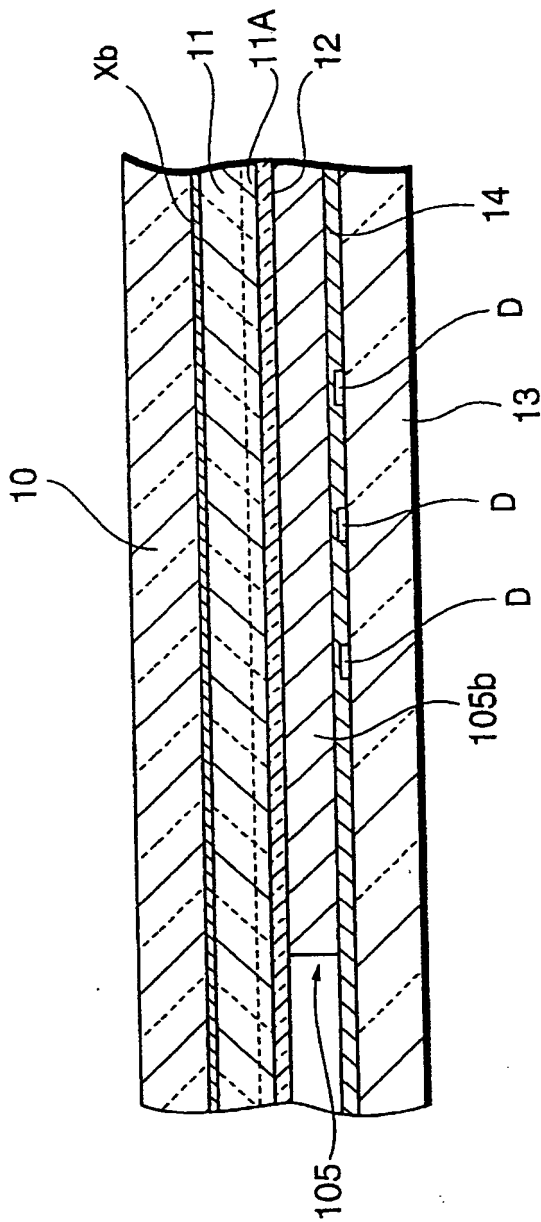


Fig. 45

W10-W10 SECTION

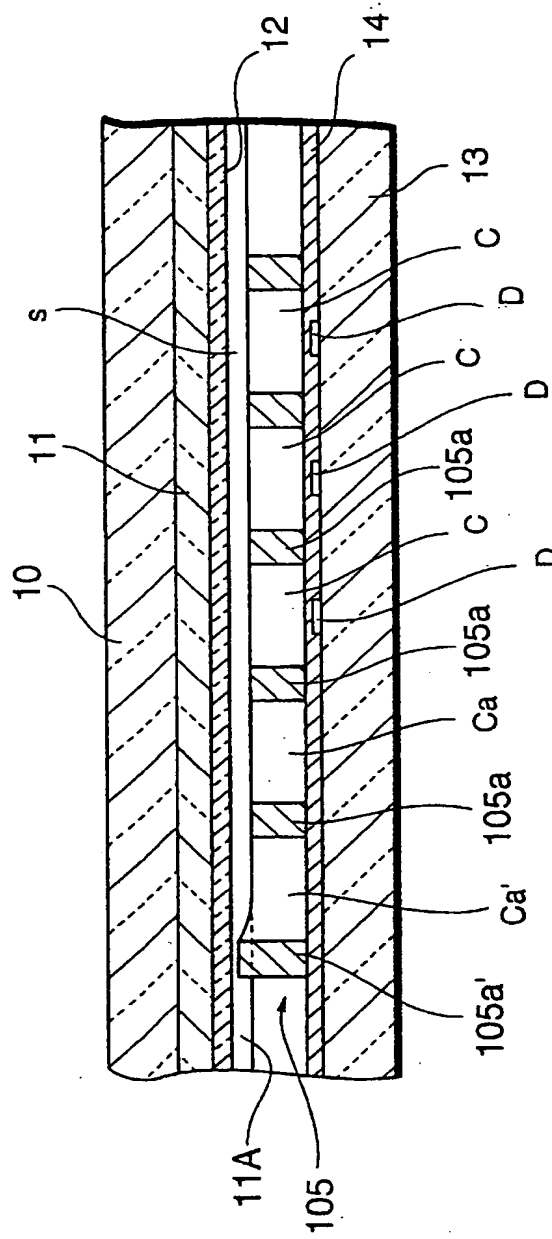


Fig. 46

V 1 3 — V 1 3 SECTION

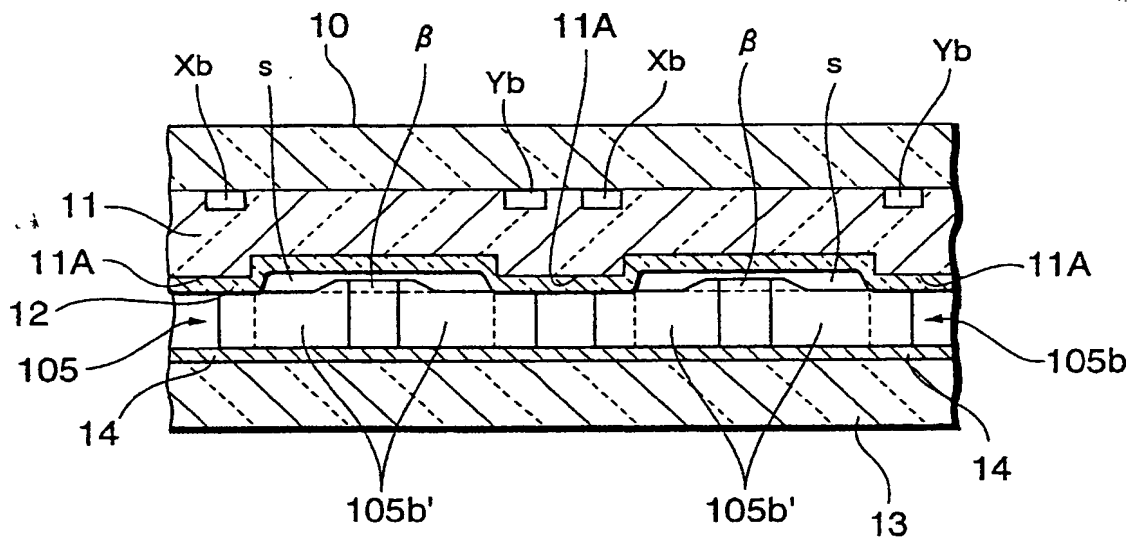


Fig.47

(PRIOR ART)

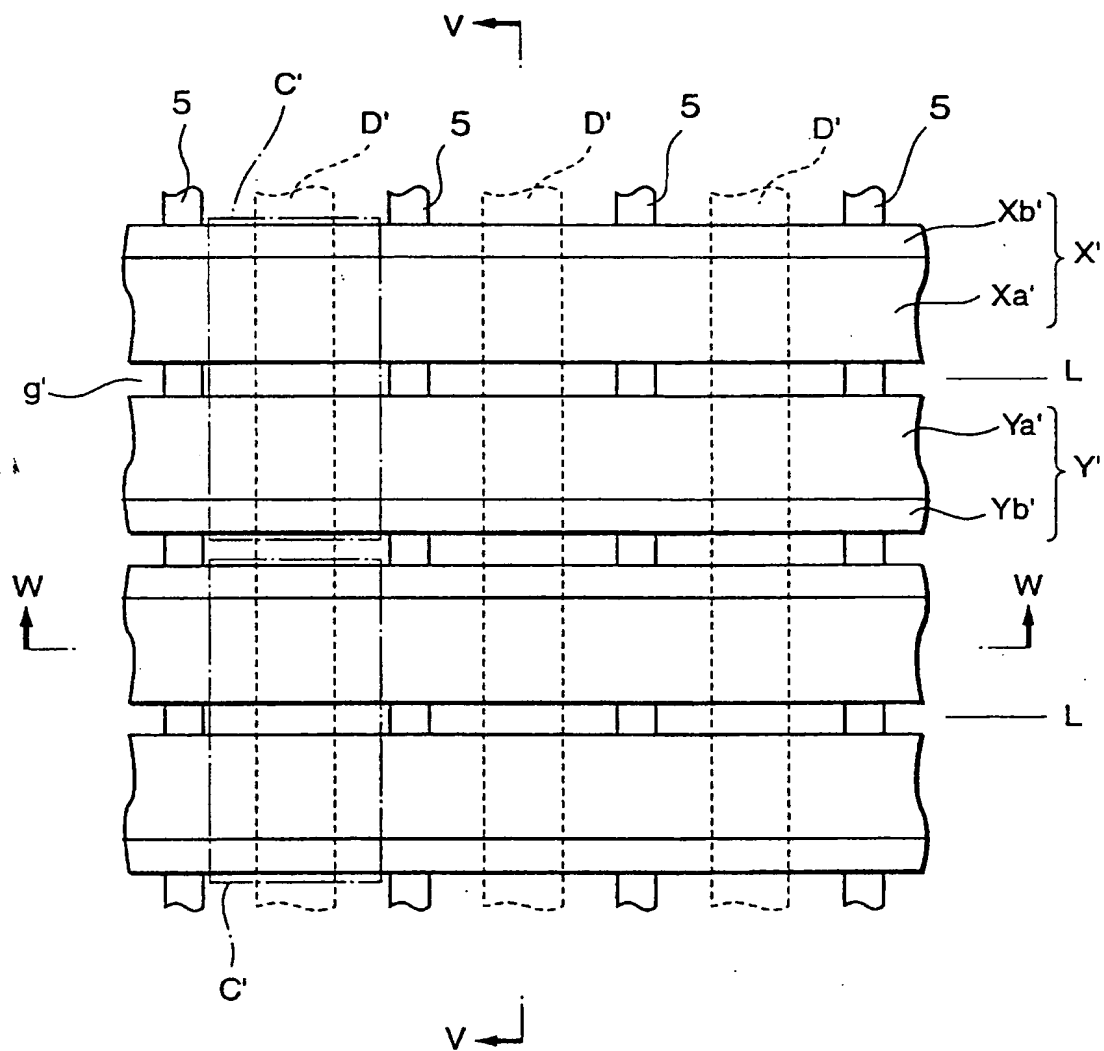


Fig.48 (PRIOR ART)

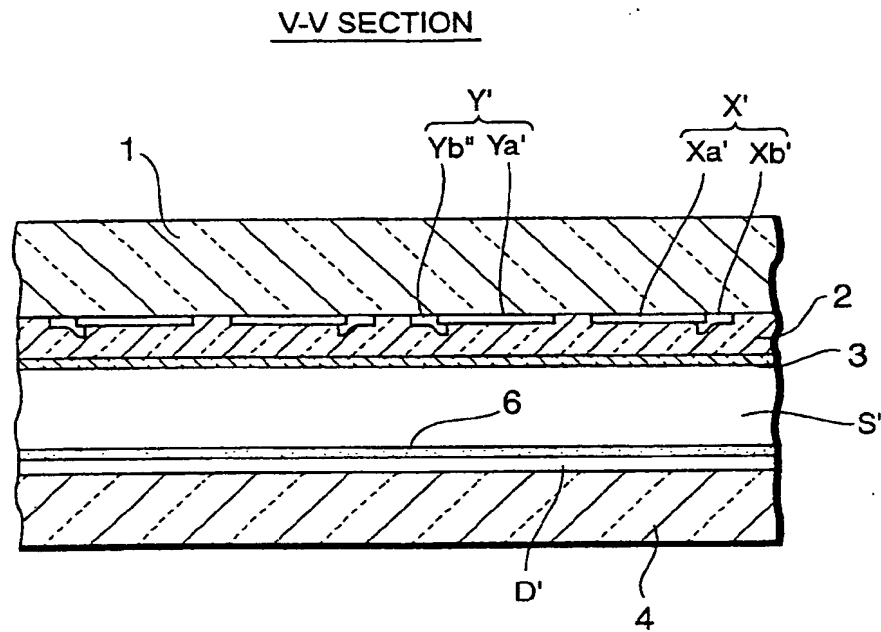
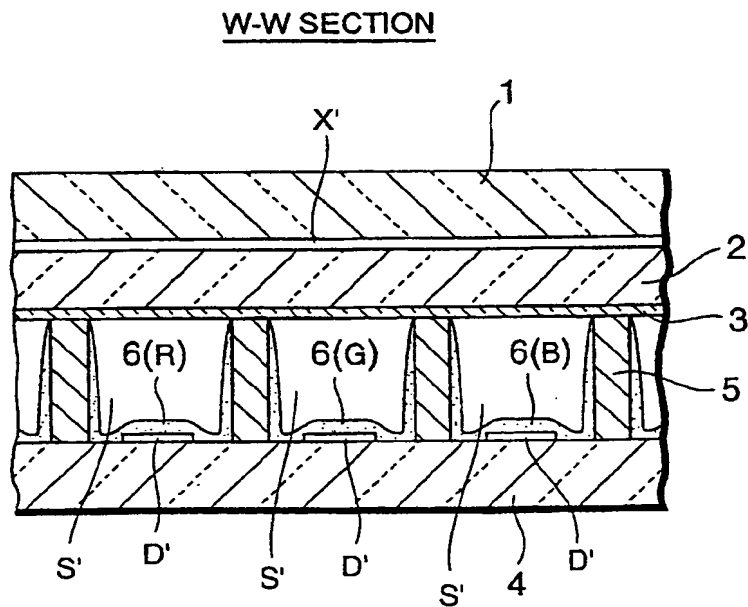
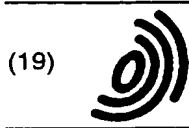


Fig.49 (PRIOR ART)





Europäisches Patentamt
European Patent Office
Office européen des brevets



(11) EP 1 017 081 A3

(12) EUROPEAN PATENT APPLICATION

(88) Date of publication A3:
28.02.2001 Bulletin 2001/09

(51) Int Cl.7: H01J 17/49

(43) Date of publication A2:
05.07.2000 Bulletin 2000/27

(21) Application number: 99126025.8

(22) Date of filing: 27.12.1999

(84) Designated Contracting States:
AT BE CH CY DE DK ES FI FR GB GR IE IT LI LU
MC NL PT SE
Designated Extension States:
AL LT LV MK RO SI

(30) Priority: 28.12.1998 JP 37312998
26.04.1999 JP 11770199
26.05.1999 JP 14637399

(71) Applicant: Pioneer Corporation
Meguro-ku, Tokyo (JP)

(72) Inventors:
• Koshio, Chiharu, c/o Pioneer Corporation
Nakakoma-gun, Yamanashi-ken 409-3843 (JP)

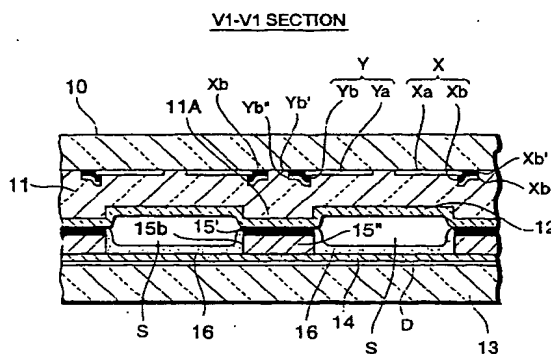
• Amemiya, Kimio, c/o Pioneer Corporation
Nakakoma-gun, Yamanashi-ken 409-3843 (JP)
• Komaki, Toshihiro, c/o Pioneer Corporation
Nakakoma-gun, Yamanashi-ken 409-3843 (JP)
• Taniguchi, Hitoshi, c/o Pioneer Corporation
Nakakoma-gun, Yamanashi-ken 409-3843 (JP)
• Sakai, Tatsuro, c/o Pioneer Corporation
Nakakoma-gun, Yamanashi-ken 409-3843 (JP)
• Masuda, Kosuke, c/o Pioneer Corporation
Nakakoma-gun, Yamanashi-ken 409-3843 (JP)

(74) Representative:
Bohnenberger, Johannes, Dr. et al
Meissner, Bolte & Partner
Postfach 86 06 24
81633 München (DE)

(54) Plasma display panel

(57) A plasma display panel comprises a front substrate (10) and a rear substrate (13), a plurality of row electrode pairs (X, Y) provided on the inner surface of the front substrate (10), a dielectric layer (11) provided on the inner surface of the front substrate (10) for covering the row electrode pairs (X, Y), a plurality of column electrodes (D) provided on the inner surface of the rear substrate (13), a partition wall assembly (15) provided between the front substrate (10) and the rear substrate (13), said partition wall assembly (15) including a plurality of longitudinal partition walls (15a) and a plurality of lateral partition walls (15b), forming a plurality of discharge cells (C). In particular, the dielectric layer (11) has a plurality of projection portions (11A) located corresponding to and protruding toward the lateral partition walls (15b) of the partition wall assembly (15), in a manner such that there would be no slots formed between the dielectric layer (11) and the lateral partition walls (15b).

Fig.2





European Patent
Office

EUROPEAN SEARCH REPORT

Application Number
EP 99 12 6025

DOCUMENTS CONSIDERED TO BE RELEVANT			
Category	Citation of documents with dates, where appropriate, of relevant passages	Relevant to claim	CLASSIFICATION OF THE APPLICATION (Int.Cl.7)
X	EP 0 823 722 A (HITACHI LTD) 11 February 1998 (1998-02-11) * column 25, line 13 - column 27, line 13; figure 12 *	1-3,30	H01J17/49
P,X	EP 0 920 048 A (HITACHI LTD) 2 June 1999 (1999-06-02) * column 20, line 13 - column 21, line 39; figures 13,14 * * column 23, line 57 - column 24, line 16 *	1-3,30	
A	PATENT ABSTRACTS OF JAPAN vol. 1995, no. 04, 31 May 1995 (1995-05-31) -& JP 07 029497 A (FUJITSU LTD), 31 January 1995 (1995-01-31) * abstract *	1,31	
A	EP 0 554 172 A (FUJITSU LTD) 4 August 1993 (1993-08-04) * column 8, line 30 - line 54; figure 4 *	1	
<p>-----</p> <p>The present search report has been drawn up for all claims</p>			<p>TECHNICAL FIELDS SEARCHED (Int.Cl.7)</p> <p>H01J</p>
Place of search		Date of completion of the search	Examiner
THE HAGUE		12 October 2000	DE RUIJTER, F
<p>CATEGORY OF CITED DOCUMENTS</p> <p>X : particularly relevant if taken alone Y : particularly relevant if combined with another document of the same category A : technological background O : non-written disclosure P : intermediate document</p> <p>T : theory or principle underlying the invention E : earlier patent document, but published on, or after the filing date D : document cited in the application L : document cited for other reasons</p> <p>& : member of the same patent family, corresponding document</p>			

EPO FORM 1503 03/02 (P04C01)



European Patent
Office

Application Number

EP 99 12 6025

CLAIMS INCURRING FEES

The present European patent application comprised at the time of filing more than ten claims.

- ☐ Only part of the claims have been paid within the prescribed time limit. The present European search report has been drawn up for the first ten claims and for those claims for which claims fees have been paid, namely claim(s):
- ☐ No claims fees have been paid within the prescribed time limit. The present European search report has been drawn up for the first ten claims.

LACK OF UNITY OF INVENTION

The Search Division considers that the present European patent application does not comply with the requirements of unity of invention and relates to several inventions or groups of inventions, namely:

see sheet B

- ☐ All further search fees have been paid within the fixed time limit. The present European search report has been drawn up for all claims.
- ☐ As all searchable claims could be searched without effort justifying an additional fee, the Search Division did not invite payment of any additional fee.
- ☐ Only part of the further search fees have been paid within the fixed time limit. The present European search report has been drawn up for those parts of the European patent application which relate to the inventions in respect of which search fees have been paid, namely claims:
- ☒ None of the further search fees have been paid within the fixed time limit. The present European search report has been drawn up for those parts of the European patent application which relate to the invention first mentioned in the claims, namely claims:

1-28, 30



European Patent
Office

**LACK OF UNITY OF INVENTION
SHEET B**

Application Number

EP 99 12 6025

The Search Division considers that the present European patent application does not comply with the requirements of unity of invention and relates to several inventions or groups of inventions, namely:

1. Claims: 1-28, 30

Partition wall assembly having two-layer structure.

2. Claims: 29,31

Each row electrode having plurality of protruding portions.

**ANNEX TO THE EUROPEAN SEARCH REPORT
ON EUROPEAN PATENT APPLICATION NO.**

EP 99 12 6025

This annex lists the patent family members relating to the patent documents cited in the above-mentioned European search report. The members are as contained in the European Patent Office EDP file on
The European Patent Office is in no way liable for these particulars which are merely given for the purpose of information.

12-10-2000

Patent document cited in search report	Publication date	Patent family member(s)	Publication date
EP 0823722 A	11-02-1998	JP 10049072 A	20-02-1998
		US 5939828 A	17-08-1999
EP 0920048 A	02-06-1999	JP 11312470 A	09-11-1999
JP 07029497 A	31-01-1995	NONE	
EP 0554172 A	04-08-1993	JP 2731480 B	25-03-1998
		JP 5205642 A	13-08-1993
		JP 3054489 B	19-06-2000
		JP 5290721 A	05-11-1993
		JP 5299022 A	12-11-1993
		JP 3007751 B	07-02-2000
		JP 5299019 A	12-11-1993
		JP 5307935 A	19-11-1993
		DE 69318196 D	04-06-1998
		DE 69318196 T	27-08-1998
		US 5674553 A	07-10-1997
		US 5661500 A	26-08-1997
		US 6097357 A	01-08-2000

EPO FORM P0459

For more details about this annex : see Official Journal of the European Patent Office, No. 12/82

THIS PAGE BLANK (USPTO)